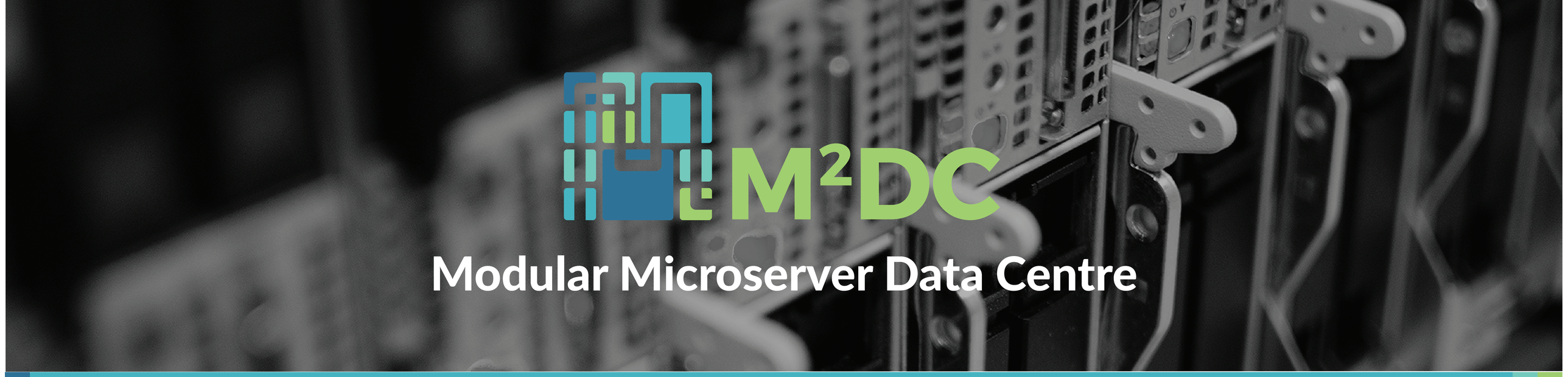


M²DC

Modular Microserver Data Centre

M2DC // www.m2dc.eu // Duration: 01.01.2016 - 31.12.2018

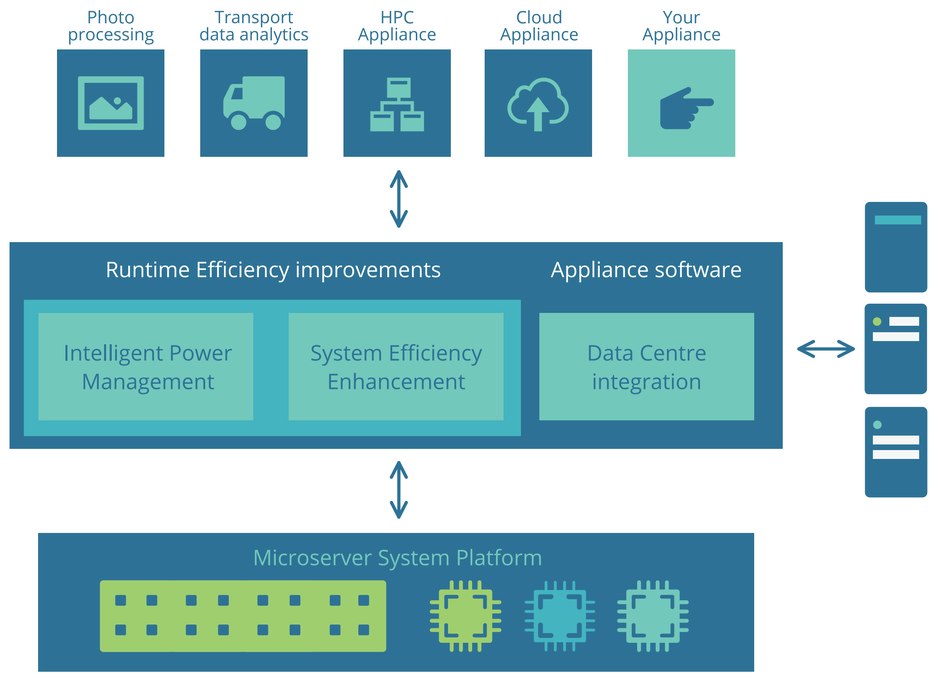
FUNDED BY
THE EUROPEAN UNION

M2DC Objectives and Status

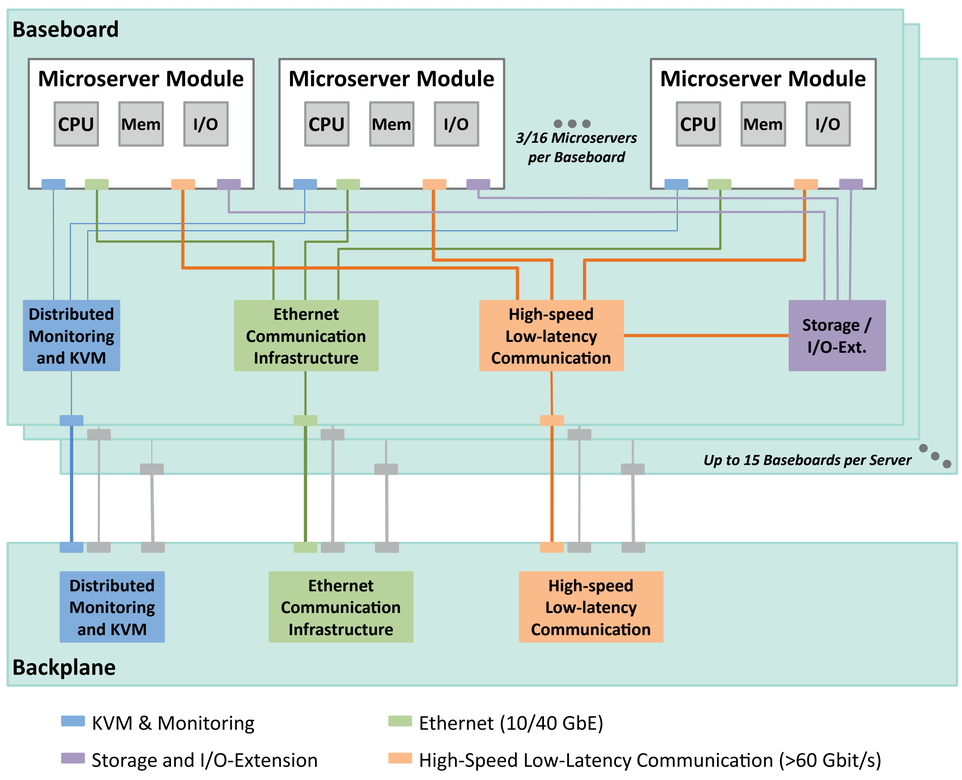
M2DC targets the development of a new class of energy-efficient TCO-optimized appliances with built-in efficiency and dependability enhancements. The appliances will be easy to integrate with a broad ecosystem of management software and fully software-defined to enable optimization for a variety of future demanding applications in a cost-effective way.

The M2DC server platform will enable customization and smooth adaptation to various types of applications, while advanced management strategies and system efficiency enhancements (SEE) will be used to achieve high levels of energy efficiency, performance, security and reliability. The M2DC middleware will provide a data centre capable abstraction of the underlying heterogeneity of the server.

First project results include new microserver designs based on ARM64 and Intel Stratix 10. Baseline benchmarks show the high potential of accelerators for the targeted applications including photo finishing systems, IoT data processing, cloud computing, CNN and HPC. In the next months we will finish the system design including an optimized middleware for deployment of the optimized appliances.



M2DC Server Communication Infrastructure



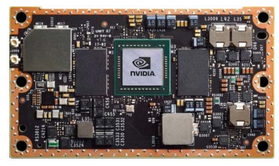
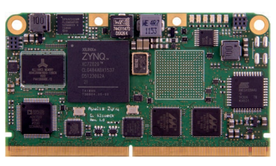
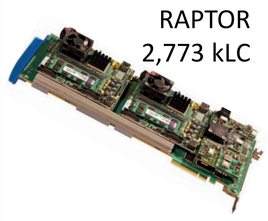
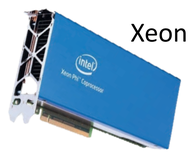
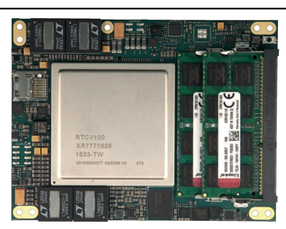
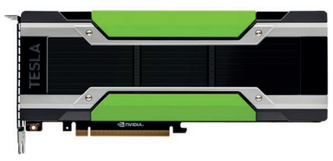
M2DC System Architecture

- Heterogeneous platform combining x86 and ARM64 CPUs, MPSoCs, GPUs and FPGAs
- High-speed, low-latency communication infrastructure, scalable across multiple M2DC servers
- Resource efficient, high dense, modular approach
- Up to 240 low-power microservers or 45 high-performance microservers per chassis
- Blade style design, hot pluggable/swappable
- Microservers based on established Computer on Module standards
  - COM Express, Nvidia Jetson, Toradex Apalis
- New microservers developed within M2DC
  - ARM64 Microserver: 32 Core Cortex-A72 @ 2.1 GHz
  - Intel Stratix 10 Microserver: Quad-core ARM Cortex-A53 and high density FPGA fabric

M2DC Software Architecture

- Our goal: Turn-key ready, easy-to use framework for appliances
- M2DC middleware stack based on OpenStack Ironic
  - Provides bare metal (micro)server software deployment and lifecycle management
  - Integration of extensions for handling the dynamic and hetero-geneous nature of the microservers and hardware accelerators
  - OpenStack extensions for dynamic node composition, combining CPU and accelerator nodes as required by the application
- Embedded fine-grained system monitoring with distributed preprocessing of sensor data (e.g., power, voltage, temperature)
- Management layer for energy and thermal aware distribution of workload on server and rack level

M2DC Microserver Overview

	CPU Microserver	GPGPU	FPGA Microserver	PCIe-Extensions
Low-Power Microserver	 NVIDIA Tegra X1/P1 4 Core A57@1.73 GHz + Maxwell GPGPU@1.5 GHz 2 Core Denver + 4 Core A57 + Pascal GPGPU@1.5 GHz		 Xilinx Zynq 7020 85 kLC	 RAPTOR 2,773 kLC  Xeon Phi  PCIe SSD
High-Performance Microserver	 ARMv8 Server SoC 32 Core A72@2.1 GHz	 NVIDIA Tesla P100 Pascal GPGPU@1.3 GHz	 Intel Stratix 10 SoC 1,092 kLC	

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