MONT-BLANC 2020

Our mission:
Trigger the development of the next generation of industrial processor for Big Data and High Performance Computing

Keeping in mind economic sustainability

Mont-Blanc 2020 includes the analysis of the requirements of other markets. The project's strategy based on modular packaging would make it possible to create a **family of SoCs targeting markets beyond conventional HPC,** such as «embedded HPC» for autonomous driving.

Project Objectives

Mont-Blanc 2020 will provide **new IPs**, such as **a new low-power mesh interconnect** based on the Coherent Hub Interface (CHI) architecture :

- supporting **up to 128 low power HPC cores;**
- each core embedding **2 vector units from 128 to 1024 bits wide;**
- interfacing HBM3 memory controllers to sustain **up to 2 TB/s** of memory bandwith.

Mont-Blanc 2020 will **demonstrate the performance** :

- Power, Performance and Area (PPA) **metrics in 7 nm**,
- **prototype implementation in RTL** for some of its key components and demonstration on an emulation platform,
- 'embedded processing' **POC on FPGA** .

3 Key Challenges

To achieve the **desired performance** with the **targeted power consumption**, the project will need to tackle these challenges :

1. understand the **trade-offs between vector length, NoC bandwith and memory bandwith** to maximize processing unit efficiency;
2. an **innovative on-die interconnect** that can deliver enough bandwith with minimum energy consumption;
3. a **high-bandwith / low power memory solution** with enough capacity and bandwith for Exascale aplications

What's next ?

Mont-Blanc 2020 is **at the heart of the European exascale supercomputer effort,** since most of the IP developed within Mont-Blanc 2020 will be reused and productized in the **European Processor Initiative (EPI)**.

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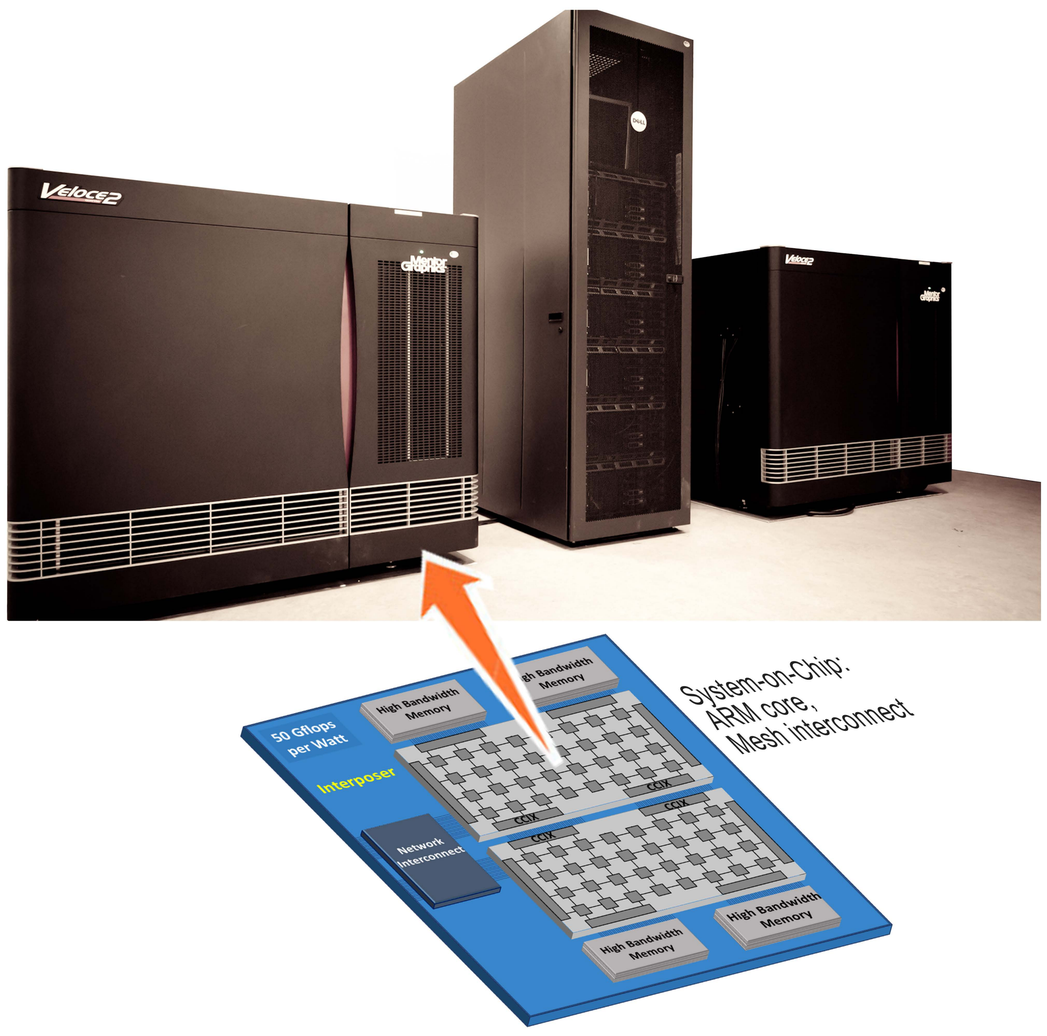
A demonstrator : from design to hardware emulation



A Key Output: the MB2020 demonstrator

The prototype will run on an emulator platform; it will be based on trace-based SVE traffic generators combined with the RTL model of the NoC and the full memory hierarchy.
Its objectives :

- **validation of the design and the associated toolchain** in the context of real-life applications,
- **cycle-accurate evaluation of performance at SoC level** that will be extrapolated to predict the impact of MB2020 designs for a full HPC system targeting Exascale computing.

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December 2017 to November 2020

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