CPU Water Cooling Temperature Effects on the Performance and Energy Consumption

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Abstract

Energy efficiency has become one of the critical elements for data center operation. Warm water cooling has been gaining increasing attention as an effective approach to reduce the power consumption, and to improve the PUE (Power Usage Effectiveness). However, CPU power consumption tends to increase as the leakage current increases with the rise in the CPU running temperature. In addition, modern CPU also possesses a dynamic frequency adjusting mechanism to reduce the clock frequency during periods of low workload, or to prevent thermal runaway and failure, which may impact the performance. In this poster, we present an own developed warm water cooled CPU evaluation environment to assist qualitative and systematic evaluations of these probable negative side-effects of the warm water cooling environment. Our investigations have mainly focused on the following points:

- Pros
 - Significantly reduce the energy consumption of cooling system
- Probable Cons
 - Decrease the computational performance (CPU frequency)
 - Increase the CPU power consumption (leakage current)
 - Increase the CPU failure rate (junction temperature)

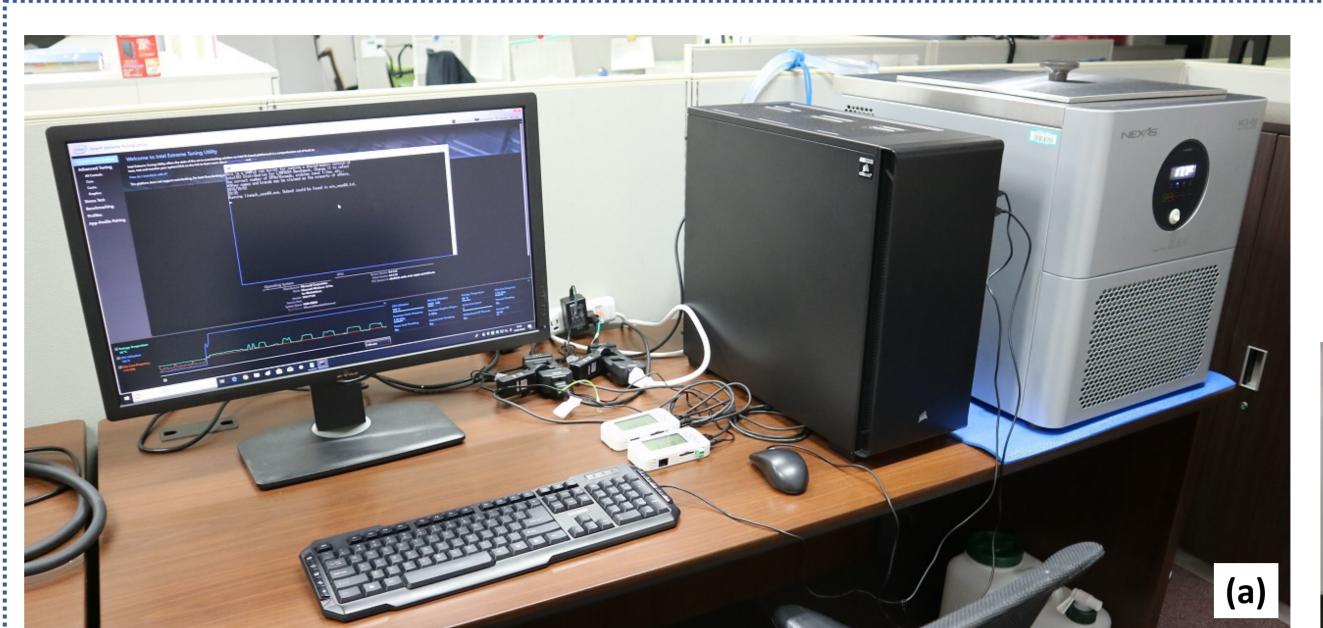






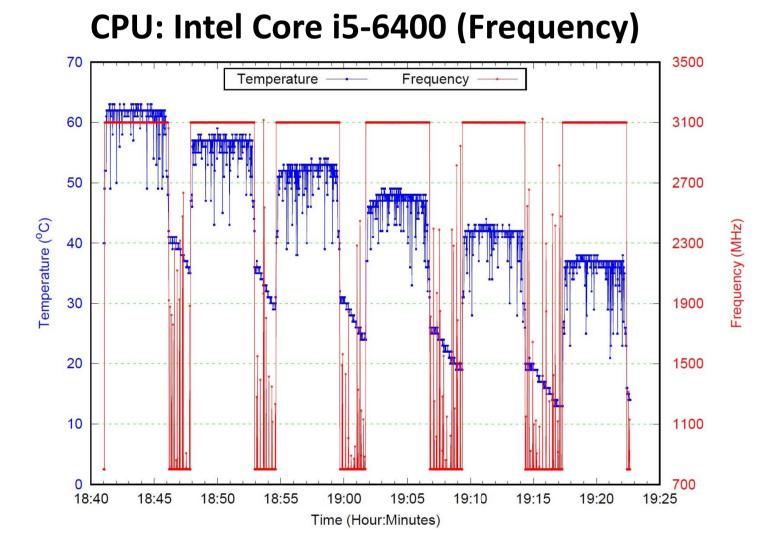
Figure 1: (a) Evaluation environment with a PC attached to a temperature controlled water circulating system (chiller & heater); (b) PC with a water cooled CPU (Skylake microarchitecture); (c) Portable power monitor and logger.

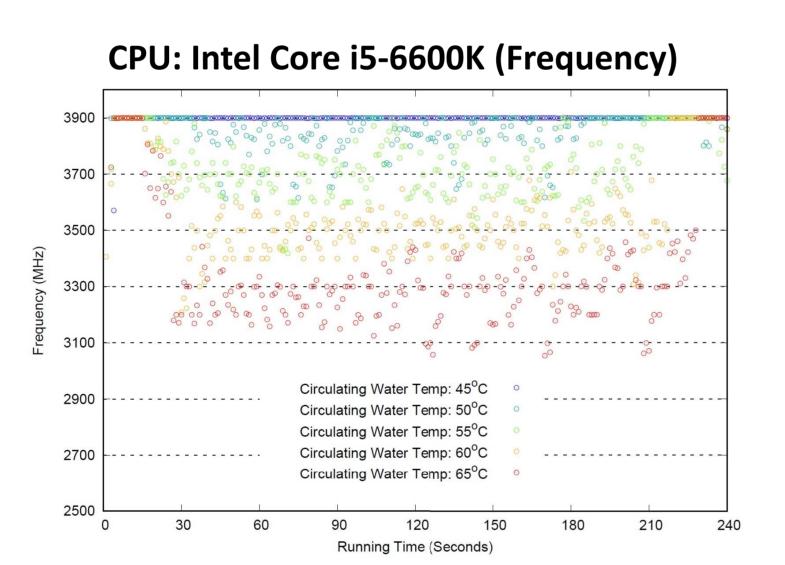
| Water Circulator | AS ONE NEXAS MCX-450 |
|-------------------|------------------------|
| Operational Range | -20°C to 90°C |
| Pump throughput | Approx. 15 liters/min. |
| Tank volume | 22 liters (MAX) |
| Chiller | 450W (at 20°C) |
| Heater | 1000W |

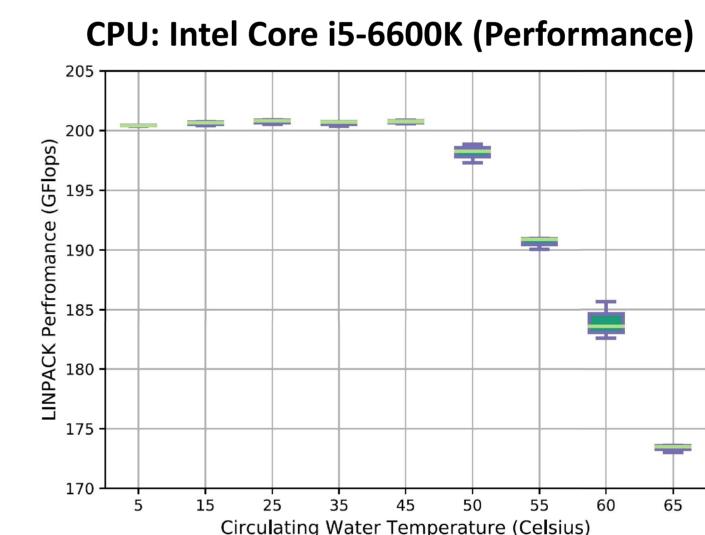
| Desktop PC | DIY PC |
|---------------|-----------------------------|
| CPU | Intel Core i5 (6400, 6600K) |
| Water Blocks | KOOLANCE (EVO, Velocity) |
| Memory | 32GB RAM (DDR4-2666) |
| HDD | 250GB (SAMSUNG SSD850 EVO) |
| Power Monitor | OMRON ZN-CTX21 |

Computational Performance

Intel Core is CPU (Skylake microarchitecture): We could observe that without reaching the CPU critical temperature, the CPU frequency remains constant, and the computational performance is not affected. Once the CPU frequency reduction (CPU throttling) occurs, the computational performance degradation is proportional to the reduction in the CPU frequency; Intel Xeon Phi CPU: The CPU frequency reduction (CPU throttling) can occur in a much lower temperature than the critical temperature (90°C).







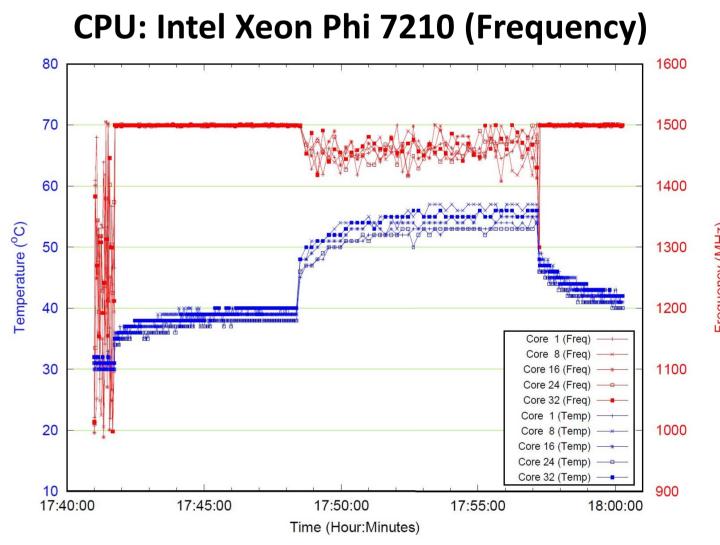
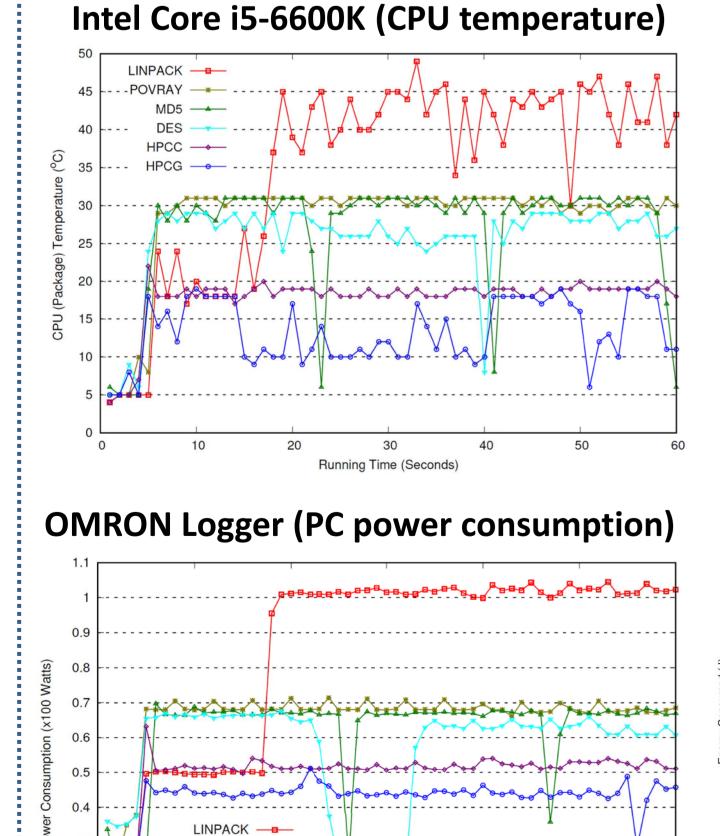
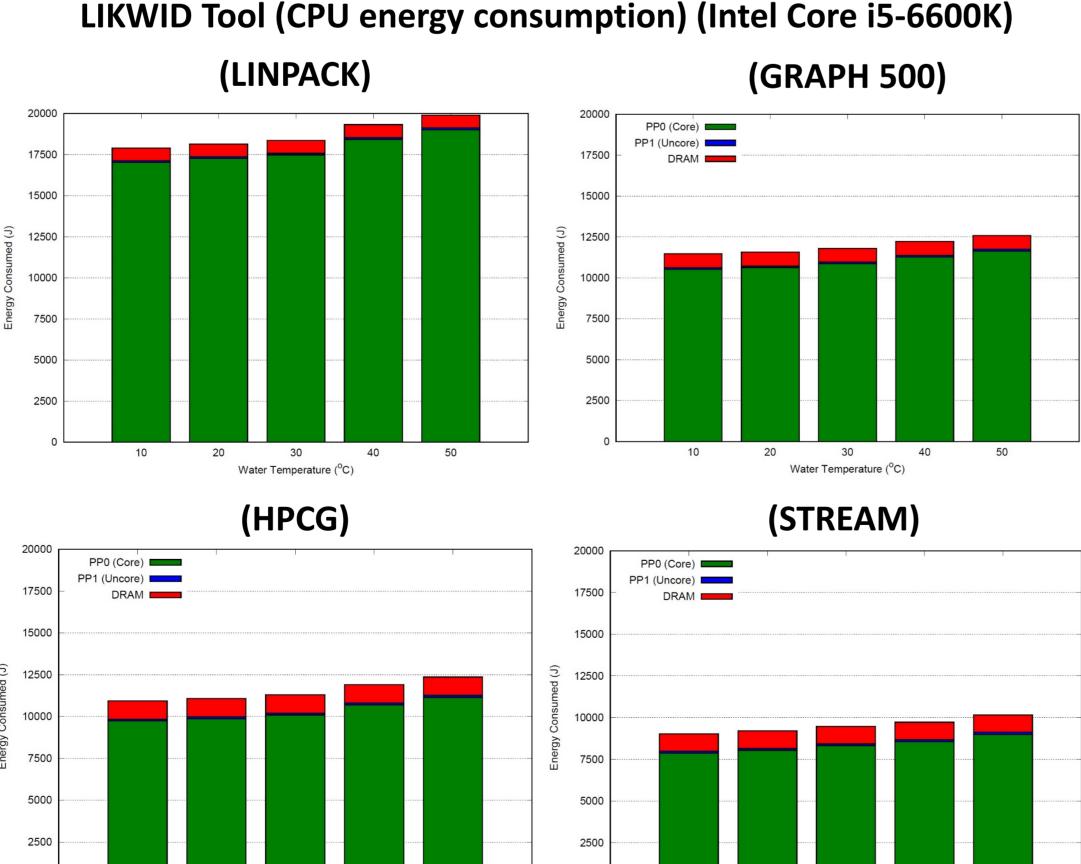


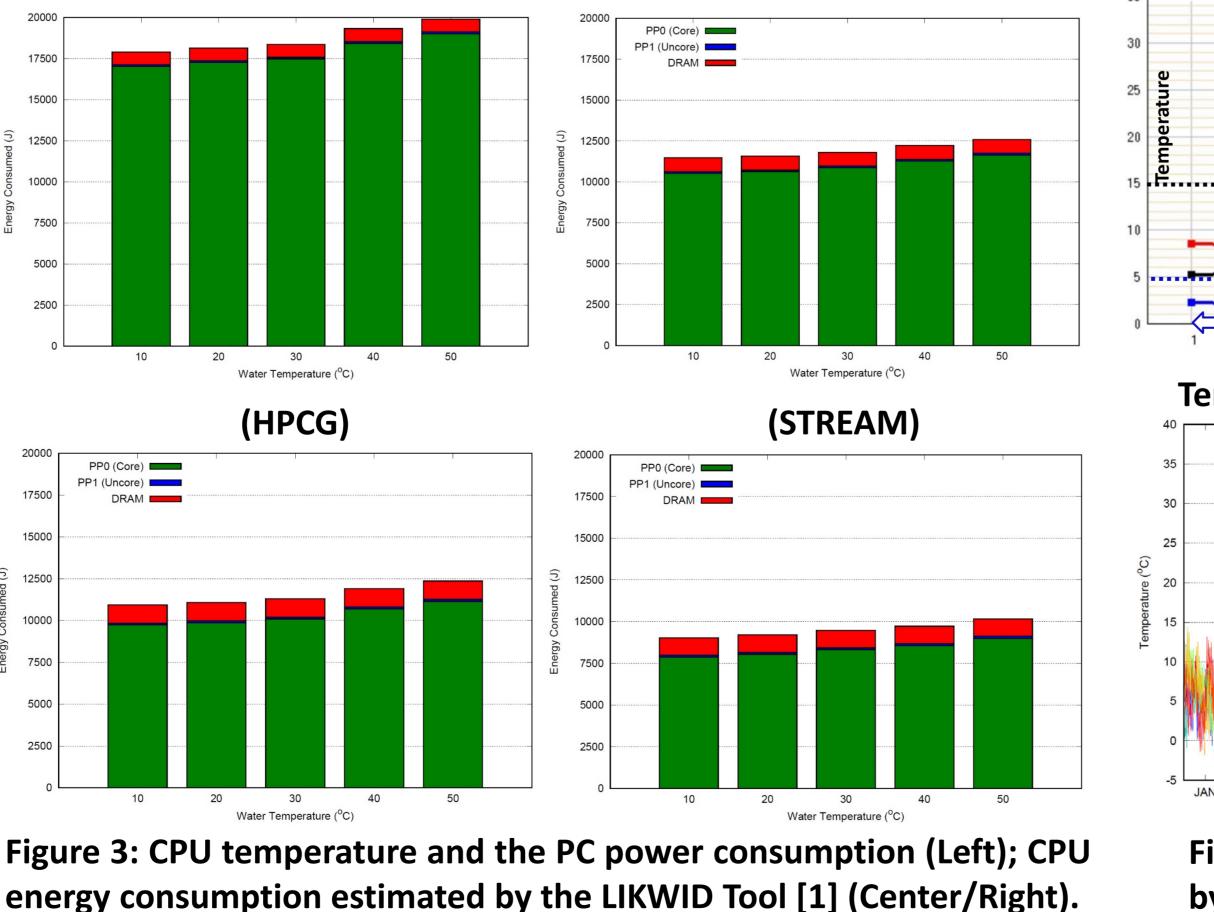
Figure 2: CPU frequency behavior below the critical temperature (Left), and when surpasses this temperature threshold (Center-Left); Computational performance degradation is directly proportional to the reduction in the CPU frequency, after reaching the critical temperature (Center-Right); CPU throttling on an Intel Xeon Phi CPU occurred below the critical temperature (Right).

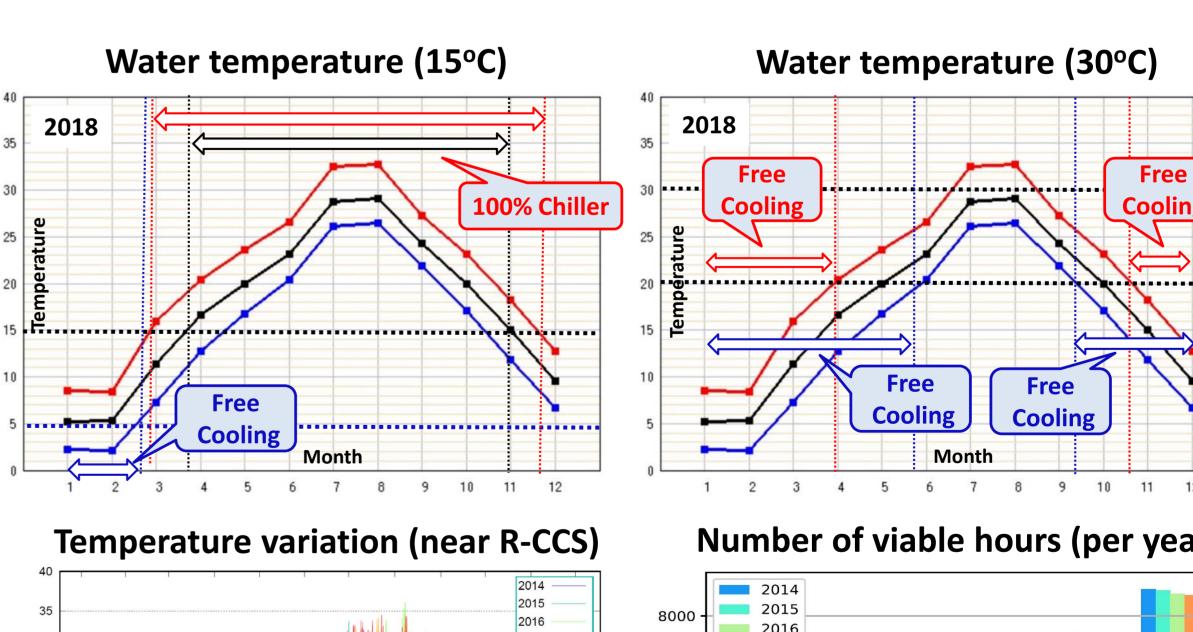
Energy Consumption

CPU: When the CPU frequency remains constant, we could observe that the power consumption almost follows the CPU temperature changing behavior as verified by running different benchmark applications. We could also observe a slight increase in the CPU energy consumption, estimated by the LIKWID Tool, when the CPU running temperature increases; Water Cooling: We have also analyzed the applicability of the free cooling method at the RIKEN R-CCS region by using the weather data from the Japan Meteorological Agency. As a case study, we used the same temperature threshold (10°C lower than the set temperature) utilized by a commercial hybrid free cooling/chiller system.









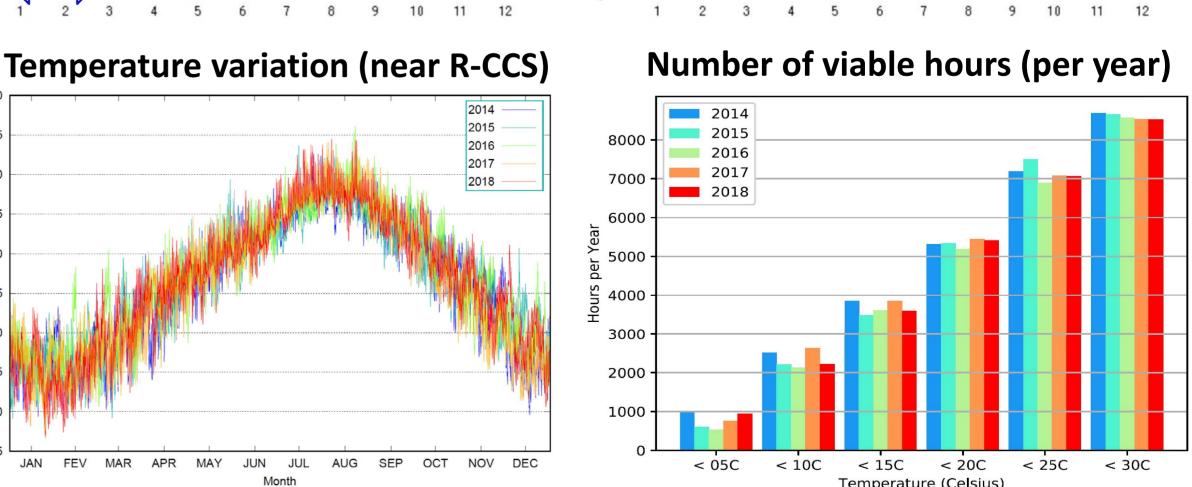


Figure 4: Applicability analysis of the free cooling method at the R-CCS by using the hourly measured local weather data ("Kobe Airport" data).

References

[1] Jan Treibig, Georg Hager, Gerhard Wellein, "LIKWID: A Lightweight Performance-Oriented Tool Suite for x86 Multicore Environments," 2010 39th International Conference on Parallel Processing Workshops, pp. 207-216, 2010.

