ISC High Performance

ISC 2019 AGENDA

FUELING INNOVATION

WELCOME TO ISC HIGH PERFORMANCE

Tutorials
Sunday, June 16, 2019

Conference & Exhibition
Monday, June 17 - 19, 2019

Workshops
Thursday, June 20, 2019

JUNE 16 - 20, 2019 I FRANKFURT, GERMANY I isc-hpc.com

Welcome to ISC High Performance 2019

Thomas and Martin Meuer

Once again, we want to welcome our attendees to the ISC High Performance conference and exhibition, an annual landmark event for the international HPC community. And it truly is international, with representation from nearly 60 countries, spread across Europe, Asia, Africa, North America, and South America. This melting pot of technical professionals and business leaders is what makes ISC High Performance such a captivating forum for sharing ideas and learning about developments in our field from around the world.

This year's theme – Fueling Innovation – is a fitting reflection of how HPC is propelling both scientific research and commercial advancements across nearly every domain. The embrace of artificial intelligence by practitioners has accelerated these developments and expanded the breadth of applications that rely on HPC. Innovation will receive additional fuel in the years ahead as exascale technologies make their way into the industry.

A prime example of how this innovation is realized will be illustrated in this year's opening keynote, The Algorithms of Life - Scientific Computing for Systems Biology, which will be delivered by Professor Ivo Sbalzarini, of TU Dresden and the Max Planck Institute of Molecular Cell Biology. In his presentation, Professor Sbalzarini will speak about how HPC is helping to develop a new understanding of how biological systems operate and their underlying mechanisms.

The opening keynote also reflects our devotion to raising the level scientific research that is presented at the conference. Our commitment to this goal and the academic program, in general, has helped make ISC High Performance a showcase for some of the best HPC-backed research in the world. The quality of the research papers and posters has improved again this year, thanks to our stringent peer review policy.

The level of innovation present in the industry is also mirrored in our exhibition, a venue for vendors and research organizations to highlight their newest products and technologies. This year, we have over 160 exhibitors, each with their own unique story to tell. Take the time to get to know how they are shaping the industry – and how they are being shaped by it.

Finally, we want to thank all the 2019 chairs and committee members for their dedication building a conference that we're extremely proud of. That starts with our Program Chair, Professor Yutong Lu, Director of National Supercomputing Center in Guangzhou, China. Professor Lu, along with our fantastic ISC Program Team, have developed an impressive program that reflects the dynamic nature of high performance computing in 2019. Our profound gratitude also extends to our contributors, sponsors, partners, and volunteers. Thank you all for making this year's conference and exhibition possible!

Best regards,

Martin Meuer and Thomas Meuer
ISC High Performance General Co-Chairs

FUELING
INNOVATION

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Monday, June 17th

Room: Kontrast
1:00 pm - 2:00 pm

The Green500: Trends in Energy Efficient Supercomputing

The Green500: Trends in Energy Efficient Supercomputing
Wu Feng (Virginia Institute of Technology, Green500), Erich Strohmaier (Lawrence Berkeley National Laboratory, Top500), Thomas R. Scogland (Lawrence Livermore National Laboratory, Green500)

With power becoming a first-order design constraint on-par with performance, it is important to measure and analyze energy-efficiency trends in supercomputing. To raise the awareness of greenness as a first-order design constraint, the Green500 seeks to characterize the energy-efficiency of supercomputers for different metrics, workloads, and methodologies. Based on this characterization, it also provides a ranking of the most energy-efficient supercomputers in the world. This BoF discusses trends across the Green500 and highlights from the current Green500 list.

In addition, the Green500, Top500, and Energy Efficient HPC Working Group have been working together on improving power measurement methodology and this BoF presents case studies from sites that have made power submissions that meet the highest quality level of measurement methodology. This highest quality level requires a full-system energy measurement and improves the accuracy and reproducibility of the information reported on the Green500 list compared to lower quality measurements.

The goals of this BoF are multi-fold: (1) analyze and announce the latest Green500 List, (2) present technical details and analysis on three of the most energy-efficient supercomputers, and (3) present case studies on improving quality and accuracy aspects of the power measurement methodology.

Room: Kontrast
2:00 pm - 3:00 pm

The HPC PowerStack: A Community-driven Collaboration Toward a Software Stack for Power and Energy Efficiency

The HPC PowerStack: A Community-driven Collaboration Toward a Software Stack for Power and Energy Efficiency

Siddhartha Jana (Energy Efficient HPC Working Group, Intel), Martin Schulz (Technical University of Munich, Leibniz Supercomputing Centre (LRZ)), Masaaki Kondo (RIKEN), Aniruddha Marathe (Lawrence Livermore National Laboratory), Ryuichi Sakamoto (The University of Tokyo)

While there exist several standalone efforts that attempt to tackle exascale power and energy challenges, the majority of the implemented techniques have been designed to meet site-specific needs. There is no consensus among the stakeholders in academia, research and industry on which software components of modern HPC stack should be deployed and how they should interoperate. Coordination among these components is critical towards maximizing a target metric (such as FLOPS per watt) while meeting operating constraints (such as energy).

This realization led to the formation of the PowerStack Community in 2016 (https://www.osti.gov/biblio/1466153/). Its charter is to identify what power optimization software actors are needed, how they interoperate to streamline the optimization goals, and how to glue together existing open source production software for a cost-effective yet cohesive, cross-platform implementation of the software stack.

This interactive vendor-neutral BoF will provide a platform to bring together the stakeholders from academia, research and industry to participate in this consortium and work towards fine-tuning the stack. The vision of this BoF is to share lessons learned through prototyping efforts, provide progress updates, invite audience feedback on current directions, brainstorm solutions to open questions, and issue a call-for-collaboration.

Room: Kontrast
4:00 pm - 5:00 pm

LUSTRE in HPC and Big Data: Status, New Features and Roadmap

LUSTRE in HPC and Big Data: Status, New Features and Roadmap

Frank P. E. Baetke (EOFS), Sarp H. Oral (ORNL, OpenSFS)

LUSTRE is the leading open source file system for HPC and now supports many HPC and AI/ML infrastructures even beyond its traditional stronghold in academia and scientific research. It has gained

wide adoption in segments like financial services, the energy sector, manufacturing, life sciences and digital content creation.

At this year's ISC BoF developers, administrators, users and solution providers will gather to discuss the current roadmap, new features, innovative developments and deployments as well as new challenges and the current status of the LUSTRE community that continues to drive LUSTRE forward. At the BoF we will focus on the recent feature developments and discuss how they will shape the next years of LUSTRE deployment around the world. Examples of important and requested features are: Small File performance improvements (Data on MDT), Erasure Coding and the ability to leverage multiple network interfaces (Multi-Rail LNet).

We will address benefits, experiences and issues with released versions up to LUSTRE 2.12.x but will also discuss features planned for releases including 2.13 scheduled for the summer of 2019. The session will start with a short introduction given by the EOFS and OpenSFS chairs about the status and structure of the LUSTRE community (including recent and upcoming community events)

The key part will be a presentation of the LUSTRE roadmap from the current release up to the end of 2020 and the related discussion topics with a special focus on the features, requirements and challenges.

Room: Kontrast
5:00 pm - 6:00 pm

BeeGFS – Architecture, Innovative Implementations and Development Plans

BeeGFS – Architecture, Innovative Implementations and Development Plans
Frank Herold (ThinkParQ), Frank Baetke (EOFS), Peter Roesch (ThinkParQ)

The open-source parallel file-system BeeGFS is one of the fastest growing middleware products for HPC and other performance-related environments. Originating as FhGFS in 2005 by the Fraunhofer Institute for Industrial Mathematics, BeeGFS (now delivered by ThinkParQ GmbH) has continued to grow and gain significant popularity in the community and has evolved into a world-wide valued filesystem offering maximum scalability, high flexibility, and robustness.

Following the success of the BeeGFS BoF at ISC 2018 which attracted around 100 attendees, this BoF will be split into three sections and the key objective is to bring developers, administrators, solution providers, and end-users together to connect, interact, discuss development plans, and share their user experiences with the product.

The BoF will begin with an overview of the latest version of the product by the architecture and development team, followed by a customer who will share experiences with an innovative implementation along with the challenges they had and have overcome since deploying BeeGFS. The architecture and development team will continue and provide an overview of the development plans of the product, where the attendees will be encouraged to interact with the speakers and provide their feedback and opinions on the product direction. All three sections of the BoF will be followed by an open Q&A with the audience.

To further prioritize what the BeeGFS users really want in the product development, there will be a quick survey at the end of the session.

Tuesday, June 18th

Room: Kontrast
8:30 am - 9:30 am

Spack Community BOF

Spack Community BOF
Todd Gamblin (LLNL), Gregory Becker (LLNL), Massimiliano Culpo (EPFL), Michael Kuhn (Universität Hamburg), Peter Scheibel (LLNL)

Spack is a package manager for scientific computing, with a rapidly growing open source community. With over 350 contributors from academia, industry, and government laboratories, Spack has a wide range of use cases, from small-scale development on laptops and clusters, to software release management for the U.S. Exascale Computing Project, to user software deployment on 6 of the top 10 supercomputer sites in the world.

At this BOF, Spack core developers will give updates on the state of the Spack community, and on new features such as environments, large-scale facility deployment, and binary package builds. A panel of Spack contributors will give 5-minute presentations on the use of Spack at their sites. Finally, we will conduct an interactive survey with the audience and open the floor for guided discussion as we review the results. All are invited to provide feedback, request features, and participate in the discussion! Help us make HPC software installation simple!

Room: Kontrast
9:30 am - 10:30 am

Unified Communication X (UCX) Community

Unified Communication X (UCX) Community
Gilad Shainer (Mellanox), Jeff Kuehn (Los Alamos National Laboratory), Pavel Shamis (Arm), Dhabaleswar Panda (Ohio State University), Brad Benton (Advanced Micro Devices), Pavan Balaji (Argonne National Laboratory), Stephen Poole (Los Alamos National Laboratory)

In order to exploit the capabilities of new HPC systems and to meet their demands in scalability, communication software needs to scale on millions of cores and support applications with adequate functionality to express their parallelism. UCX is a collaboration between industry, national labs and academia that consolidates multiple technologies that provides a unified open source framework. The UCX project is managed by the UCF consortium (http://www.ucfconsortium.org/) and includes members from LANL, ORNL, ANL, Ohio State University, AMD, ARM, IBM, Mellanox, NVIDIA and more. The session will serves as the UCX community meeting, and will introduce the latest development and specification to HPC developers and the broader user community.

High-level programming models for communication (e.g., MPI, SHMEM) can be built on top of middleware, such as Portals, GASNet, UCCS, and ARMCI or use lower-level network-specific interfaces, often provided by the vendor. While the former offer high-level communication abstractions and portability across different systems, the latter offer proximity to the hardware and minimize overheads related to multiple software layers. An effort to combine the advantages of both is UCX, a communication framework for high-performance computing systems.

UCX has already been integrated with upstream of Open MPI project and OpenSHMEM, being used with MPICH and more. UCX is now being deployed with the US DOE Coral systems. The session will enable a dialog on the future plans for UCX and review the operations of the UCX consortium. It will include performance evaluation based on testing results conducted on several US DoE systems.

Room: Kontrast
10:30 am - 11:30 am

Emerging Filesystem Technologies and Use Cases for AI and HPC

Emerging Filesystem Technologies and Use Cases for AI and HPC
Ronald Hawkins (San Diego Supercomputer Center / University of California San Diego), Dave Hiatt (WekaIO)

The goal of this BOF is to engage system managers, system administrators, users, and other interested

parties in a discussion of technologies and information exchange on best practices and lessons learned for implementing emerging, flash-based storage and file-system technologies within HPC systems. Many universities, corporations and research centers operate HPC clusters using a conventional architecture of interconnected compute nodes with minimal on-node storage coupled to a hard-drive- based (or perhaps, flash-based) parallel file system. Over the past decade, the workload on many systems has broadened from traditional modeling & simulation tasks to data-intensive analytics, machine learning, and AI. Often these new workloads exhibit I/O patterns that are not well served by the traditional parallel file system architectures. The declining cost curve of flash storage technologies, along with the emergence of new standards such as NVMe, and new implementation architectures such as hyper- converged file systems, offer the opportunity to incorporate new I/O subsystems or tiers featuring high performance random access and small block/small file I/O. This BOF will bring together interested parties in an active, discussion-oriented format to exchange ideas, experiences and share knowledge on the deployment of these new technologies in high performance computing and AI environments.

Room: Substanz 1, 2
11:00 am - 12:00 pm

InfiniBand In-Network Computing Technology and Roadmap

InfiniBand In-Network Computing Technology and Roadmap
Gilad Shainer (Mellanox Technologies), Daniel Gruner (University of Toronto), Richard Graham (Mellanox Technologies), Ron Hawkins (San Diego Supercomputing Center)

The past focus for smart interconnects development was to offload the network functions from the CPU to the network. With the new efforts in the co-design approach, the new generation of smart interconnects will also offload data algorithms that will be managed within the network, allowing users to run these algorithms as the data being transferred within the system interconnect, rather than waiting for the data to reach the CPU. This technology is being referred to as In-Network Computing. In-Network Computing transforms the data center interconnect to become a “distributed CPU”, and “distributed memory”, enables to overcome performance walls and to enable faster and more scalable data analysis.

HDR 200G InfiniBand In-Network Computing technology includes several elements - Scalable Hierarchical Aggregation and Reduction Protocol (SHARP), a technology that was developed by Oak Ridge National Laboratory and Mellanox and received the R&D100 award, smart Tag Matching and rendezvoused protocol, and more. These technologies are in use at some of the recent large scale supercomputers around the world, including the top TOP500 platforms.

The session will discuss the InfiniBand In-Network Computing technology and testing results from DoE

systems, Canada's fastest InfiniBand Dragonfly based supercomputer at the University of Toronto, the world's first HDR 200G InfiniBand systems and more.

As the needs for faster data speed accelerates, the InfiniBand Trade Association has been working to set the goals for future speeds, and this topic will also be covered at the session.

Room: Kontrast
11:30 am - 12:30 pm

Integration of HPC & AI

Integration of HPC & AI
David Brayford (LRZ), Sofia Vallecorsa (CERN openlab), Michael Steyer (Intel), Atanas Atanasov (Intel)

The upsurge in interest in the use of AI from the research community and industry to tackle "real world" problems requires HPC resources to efficiently compute and scale these complex algorithms across thousands of nodes. Unfortunately, typical data scientists are not familiar with the unique requirements and characteristics of HPC environments. They usually develop their applications with high level scripting languages or frameworks such as TensorFlow and installation processes connect to external systems and download the open source software during the build. HPC environments, on the other hand, are often based on closed source applications that incorporate parallel and distributed computing API's such as MPI and OpenMP, while users have restricted administrator privileges, and face security restrictions such as not allowing access to external systems. This BoF aims to bring together contributors, data scientists, system administrators, architects, and developers interested in the integration of AI & HPC. We propose to discuss the issues associated with the deployment of AI frameworks in a traditional HPC environment and potential solutions that enable us to successfully deploy AI frameworks on large scale HPC production systems.

Room: Substanz 1, 2
1:45 pm - 2:45 pm

The IO-500 and the Virtual Institute of I/O

The IO-500 and the Virtual Institute of I/O
Julian Kunkel (University of Reading), Jay Lofstead (Sandia National Laboratories), John Bent (DDN), George S. Markomanolis (Oak Ridge National Laboratory)

Evolving and new storage technologies introduced over the last few years are causing increasing complexity for HPC data management. Hence, analyzing, comparing, or even predicting the performance of different HPC machines and storage systems has become more complicated. To address this challenge, the community developed a benchmark that lead to the creation of the competitive IO-500 list. The benchmark consists of several data and metadata benchmarks to identify performance boundaries for optimized and suboptimal applications. In addition to offering different ways to compare storage systems, the list collects information about storage system design to help system designers make informed trade-offs when specifying new storage requirements.

The development of the benchmark is powered by the Virtual Institute for I/O (http://vi4io.org), which provides a platform for I/O enthusiasts for exchanging information, fosters international collaboration in the field of high-performance I/O, and tracks the deployment of large storage systems by hosting comprehensive information about high-performance storage systems.

The general purpose of this BoF is to foster the storage community in understanding the performance characteristics of HPC storage. The session leaders will give a series of brief talks that seed the subsequent discussions: 1) The release of the new IO-500 list and highlights. Observed issues are sketched and alternatives to overcome these are discussed with the community. 2) The virtual institute and the comprehensive data center list. 3) Roadmaps with features are sketched inviting the community to prioritize the features. The outcome of this BoF will steer the direction of these community efforts.

Room: Kontrast
1:45 pm - 2:45 pm

Multi-Level Memory and Storage for HPC, Data Analytics & AI

Multi-Level Memory and Storage for HPC, Data Analytics & AI
Hans-Christian Hoppe (Intel Datacenter Group), Michèle Weiland (Edinburgh Parallel Computing Centre), Kathryn Mohror (Lawrence Livermore National Laboratory)

Recent progress in storage-class memory (SCM) technologies combined with emerging workloads mixing HPC simulations with big data processing or AI does create a perfect opportunity for innovative HPC systems embracing SCM. These will substantially improve delivered performance, scalability and energy efficiency for data-oriented HPC codes as well as “mixed” applications, and can play a large role in removing the “I/O wall” when moving to Exascale class systems.

At the same time, significant progress has been made on memory and storage devices with increasing

capacities and performance, many of them non-volatile by nature, and systems with multiple memory and/or storage levels are becoming state-of-the-art. This presents a perfect opportunity for addressing the traditional Exascale “I/O gap” and at the same time provide the emerging breed of combined HPC and AI applications with a solid and highly performing memory/storage platform.

This BoF continues the series of successful similar sessions at ISC; it will bring together technology providers, application and system SW developers, and system operators to discuss use cases and requirements for next-generation multi-level storage/memory systems, present proof of concept prototype results, and examine the system SW and tools development.

Room: Substanz 1, 2
2:45 pm - 3:45 pm

18th Graph500 List

18th Graph500 List
Richard Murphy (Micron Technology, Inc.), David Bader (Georgia Tech), Peter Kogge (University of Notre Dame), Andrew Lumsdaine (Pacific Northwest National Laboratory), Anton Korzh (Micron Technology, Inc.), Torsten Hoefler (ETH Zurich)

Data intensive supercomputer applications are increasingly important workloads, especially for “Big Data” problems, but are ill suited for most of today’s computing platforms (at any scale!). The Graph500 list has grown to over 235 entries and has demonstrated the challenges of even simple analytics. The new SSSP kernel introduced at SC17 has increased the benchmark’s overall difficulty. Backed by a steering committee of 30 international HPC experts from academia, industry, and national laboratories, this effort serves to enhance data intensive workloads for the community. This BOF will unveil the 18th Graph500 list, expand on the new second kernel, and enhance the new energy metrics the Green Graph500. It will offer a forum for community and provide a rallying point for data intensive supercomputing problems. In this BOF we will explore emerging streaming graph applications and the potential for a new tensor benchmark, the results from the new kernel, the creation of a larger community infrastructure for analytics benchmarks and analysis, and the results of the latest list. Graph500 is the first serious approach to complement the Top 500 with data intensive applications.

Room: Kontrast
2:45 pm - 3:45 pm

Scalable Deep Learning for Industrial and Research Applications

Scalable Deep Learning for Industrial and Research Applications
Lucas A. Wilson (Dell EMC), Antonio Cisternino (University of Pisa), Valeriu Codreanu (SURFaara)

The Scalable Deep Learning for Industrial and Research Applications BoF will explore and discuss training and deployment of deep learning (DL) models across various industrial and research domains. Invited presentations will help to establish the current state of deep learning research and application to scientific and industrial projects, and provide a catalyst for what we hope to be an interesting and important conversation about the direction and potential of using deep learning.

We invite anyone interested in DL model development, deployment, infrastructure or hardware to discuss the need or desire to apply DL in businesses or research projects, the technical challenges faced when implementing DL-based solutions, the potential value DL-based solutions have provided or may provide, lessons learned in adding deep learning to existing data center operations and applications workflows, and desires for addressing current gaps and future needs.

Room: Analog 1, 2
3:45 pm - 4:45 pm

OpenMP* 5.0 is here: What do I Need to Know About it and What's Coming Next?

OpenMP* 5.0 is here: What do I Need to Know About it and What's Coming Next?
James H. Cownie (Intel Corporation (UK) Ltd), Michael Klemm (OpenMP ARB, Intel), Bronis R. de Supinski (OpenMP ARB, Livermore Computing), Barbara Chapman (cOMPunity, Stony Brook University), Simon McIntosh-Smith (University of Bristol), Christian Terboven (Aachen University), James Beyer (NVidia)

OpenMP is the most popular way in which HPC codes exploit shared memory parallelism. OpenMP 5.0 has extended that support to include a comprehensive, vendor neutral, way to describe offloading computation to attached accelerators, as well as adding enhancements to the support for CPUs.

This BoF will provide you with the information you need to understand the new standard, as well as giving you the opportunity to question OpenMP experts, many of whom were involved in defining the standard.

After short (3 minutes maximum) presentations from the experts, most of the BoF time will be used for open discussion of questions from the audience.

If you want to improve your knowledge of modern OpenMP, and understand how its new features can be

useful to you, you should attend this BoF.

Room: Substanz 1, 2
3:45 pm - 4:45 pm

International HPC Certification Program

International HPC Certification Program
Julian Kunkel (University of Reading), Weronika Filinger (Edinburgh Parallel Computing Centre (EPCC), The University of Edinburgh), Anja Gerbes (Goethe University of Frankfurt), Kai Himstedt (University of Hamburg)

The HPC community has always considered the training of new and existing HPC practitioners to be important to its growth. However, as the community becomes more diverse the traditional HPC training approaches are being challenged. The constantly growing group of users with very specific training needs, often coming from traditionally non-HPC disciplines, makes it difficult for HPC centres to identify and overcome their knowledge gaps. Most of the readily available training materials are not comprehensive and don't have clearly defined pre-requisites or learning outcomes. So how should intermediate HPC users identify the content they have not mastered yet?

There is a generally accepted set of skills required to efficiently use HPC resources, and the main goal of the International HPC Certification program is to categorise, define and eventually test them. Making clear what skills are required or recommended for specific user roles and scientific domains would benefit both the HPC service providers and practitioners.

In this BoF, speakers from academia and science present the current status and discuss the value of the approach and gather valuable feedback on the current state of the skill tree through small group discussions. The initiative received a lot of attention at ISC'18 and SC'18 and attracted a number of collaborations (including ACM SIGHPC Education Chapter). To make sure the program becomes a community-wide and sustainable effort more involvement from the HPC training community is needed. We invite anyone experienced or interested in HPC teaching and training to participate in those discussions and get involved.

Room: Kontrast
3:45 pm - 4:45 pm

Artificial Intelligence and Performance

Artificial Intelligence and Performance

Felix Wolf (TU Darmstadt), Christoph Angerer (NVIDIA), Andreas Gocht (Technical University Dresden), Torsten Hoefler (ETH Zurich), Janis Keuper (Fraunhofer ITWM), Allen Malony (University of Oregon), Ana Lucia Varbanescu (University of Amsterdam)

Artificial intelligence, and more specifically neural-network based machine learning, has evolved in leaps and bounds, and is expanding from its original constituency of vision, perception and natural language processing into many scientific fields. At the same time, computational complexity and data volumes of AI applications (in particular of training phases) increasingly outgrow the capabilities of single-node systems, and optimizing end-to-end performance becomes a key issue ("Performance for AI") .

At the same time, the proven capability of AI techniques to analyze high-dimensional data, recognize complex patterns and solving difficult optimization problems promises to substantially improve the capabilities of large scale, parallel performance analysis and of automatic code tuning. ML-based analysis functionality has been integrated into parallel performance tools, and the role of AI-directed decisions in compilation and auto-tuning systems are active research topics ("AI for performance").

This BoF brings together expert AI technology and application developers with HPC application and tool developers and end-users to investigate status quo and opportunities both in "Performance for AI" and "AI for performance", and discuss how to accelerate mutual progress.

Wednesday, June 19th

Room: Konstant
8:30 am - 9:30 am

OpenHPC Community BoF

OpenHPC Community BoF

Karl Schulz (University of Texas), David Brayford (Leibniz Supercomputing Centre), Adrian Reber (Red Hat)

This BoF aims to bring together contributors, system administrators, architects, and developers using or interested in the OpenHPC community project (http://openhpc.community). This BoF proposal is a follow-on to successful OpenHPC BoFs at ISC 2016/2017, and a pre-cursor BoF at ISC in 2015 that helped motivate creation of the OpenHPC project.

Launched in November 2015, OpenHPC is a Linux Foundation collaborative project comprised of over 35 members from academia, research labs, and industry. OpenHPC is focused on providing HPC-centric package builds for a variety of common components in an effort to minimize duplication, implement integration testing to gain validation confidence, and provide a platform to share configuration recipes from a variety of sites. To date, the OpenHPC software stack aggregates over 85 components ranging from administrative tools like bare-metal provisioning and resource management to end-user development libraries that spawn a range of scientific/numerical uses. OpenHPC adopts a familiar package repository delivery model and the BoF will begin with technical presentations from members of the OpenHPC Technical Steering Committee (TSC) highlighting current status, recent changes, and near-term roadmaps. Open discussion will follow after the update overview and this BoF will provide an opportunity for attendees to interact with members of the OpenHPC TSC and other community members to provide feedback on current conventions, ongoing packaging efforts, request additional desired components and configurations, and discuss general future trends. Feedback from attendees has been very beneficial in the past and helps prioritize and guide future community releases and long-term directions or the project.

Room: Konstant
9:30 am - 10:30 am

Data-Centric Computing for the Next Generation

Data-Centric Computing for the Next Generation
Julian Kunkel (University of Reading), Jay Lofstead (Sandia National Laboratories), Jean-Thomas Acquaviva (DDN)

The efficient, convenient, and robust execution of data-driven workflows and enhanced data management are key for productivity in scientific computing and computer-aided RD&E. Big data tools integrate compute and storage capabilities into a holistic solution demonstrating the benefit of tight integrating while the HPC community still optimizes the compute and storage components independently from each other, and, moreover, independently from the needs of end-to-end user workflows that ultimately lead to insight. Even within a single data center, utilizing homogeneous storage and compute infrastructure efficiently is complex for experts. The efficient management of data and compute capabilities in a heterogeneous environment, however, is an unresolved question as the execution of individual tasks from workflows may benefit from alternative hardware architectures and infrastructures.

In this BoF, we bring the community together to discuss visions for a data-centric compute environment of the future that gives the fastest time to insight by applying concepts like smart scheduling and compiler technology which, e.g., minimize data movement for the entire workflow and exploit capabilities of

heterogeneous environments that stretch beyond a single data center. As this has implications on data-center planning, hardware/software infrastructure starting from a higher-level workflow formulation to smarter hardware and software layers, it affects the wider HPC community. We gathered a range of stakeholders from industry and academia interested in this approach with the ultimate goal is to establish a forum that addresses the need for Next Generation Interfaces that defines and realizes the vision that will impact the next generations of scientists.

Room: Konstant
10:30 am - 11:30 am

Building Energy Efficient HPC Systems

Building Energy Efficient HPC Systems
Michael Ott (Leibniz Supercomputing Centre), Maike Gilliot (ETP4HPC, Teratec), Julita Corbalan (Barcelona Supercomputing Center, Polytechnic University of Catalonia), Peter Hopton (Iceotope)

Energy efficiency is one of the most pressing issues for HPC in general and particularly on the path to Exascale. It has to be addressed at multiple levels: applications, system software, hardware, and infrastructure. With this in mind, the ETP4HPC has forged a working group on the topic to create awareness about latest research and developments on energy efficiency in HPC, share experiences, and to promote best practices on the design and use of HPC systems and infrastructures. This BoF is organized by the ETP4HPC Energy Efficiency Working Group to allow the community to present their activities towards energy efficiency in HPC and to serve as a forum to bring together like-minded people to discuss ideas, share experiences, and outline further research topics.

Room: Konstant
11:30 am - 12:30 pm

Software Engineering and Reuse in Computational Science and Engineering

Software Engineering and Reuse in Computational Science and Engineering
David E. Bernholdt (Oak Ridge National Laboratory), Mozhgan Kabiri Chimeh (University of Sheffield), Anshu Dubey (Argonne National Laboratory, University of Chicago), Carina Haupt (DLR German Aerospace), Michael A. Heroux (Sandia National Laboratories, St. John's University), Catherine Jones (Science and Technology Facilities Council), Guido Juckeland (Helmholtz-Zentrum Dresden-Rossendorf (HZDR)), Jared O'Neal (Argonne National Laboratory), Jurriaan H. Spaaks (Netherlands eScience

Center)

Software engineering (SWE) for computational science and engineering (CSE) is challenging, with ever-more sophisticated and higher fidelity simulations of ever-larger and more complex problems involving larger data volumes, more domains, and more researchers. Targeting both commodity and custom high-end computers and the recent rise in accelerators multiplies these challenges. We invest a great deal in creating these codes, but rarely talk about that experience; we just focus on the results.

Further, the digitalization of the whole scientific process increases the attention others may give to the CSE software we produce. Transparency and reproducibility of research puts software front and center, along with concerns about its quality and longevity. With software as an increasingly important output from scientific research, there are also concerns about how to give appropriate credit in publications and for professional advancement.

Our goal is to raise awareness of SWE for CSE on supercomputers as a major challenge, and to develop an international “community of practice” to continue these important discussions outside of workshops and other “traditional” venues.

This BoF provides an opportunity for people concerned about this topic to share existing activities, discuss how we can expand and improve on them, and share the results. Presentations and discussion notes will be made available to the community at the BoF series website, http://bit.ly/swe-cse-bof.

Room: Analog 1, 2
1:45 pm - 2:45 pm

ARM for HPC: A New Era for Co-Design Opportunities

ARM for HPC: A New Era for Co-Design Opportunities
Stephen Poole (Los Alamos National Laboratory), Jeffrey Young (Georgia Institute of Technology), Oscar Hernandez (Oak Ridge National Laboratory)

In recent years, systems based on the ARM architecture have gained traction in the HPC community as evidenced by several ARM-based projects including the Japanese Post-K Computer, Sandia’s Astra system, UK’s GW4/EPSRC efforts and Europe’s “Mont-Blanc” project. ARM is now a major player in the HPC field, by introducing new technologies for HPC workloads like ARMv8-A Scalable Vector Extension (SVE) technology and related compilers and scientific libraries. To complement this increase in ARMv8 HPC systems, we want to discuss what co-design opportunities ARM brings to the table for end-users both in the context of hardware design space exploration as well as with software/hardware co-design. In

this BoF we will discuss/identify the key technologies that the HPC user community can help to co-design to have an impact on future ARM HPC systems. For example, what opportunities do we have to co-design ARM/interconnect support with low-level communication APIs (e.g. UCX, etc), how can SVE be used and extended, and how should new 3D stacked memories be used with future ARM memory subsystem? This BoF will discuss these areas and also explore user tools like emulators and simulators to explore such software and hardware co-design. We will focus on user-experiences with existing co-design tools and also feature an interactive section of the BoF to get feedback on community needs and to define proposed new applications which might be enabled by new HW, SW, and network designs or tools.

Room: Konstant
1:45 pm - 2:45 pm

Leveraging Mixed Precision and Emerging Low Precision Operators in HPC Application

Leveraging Mixed Precision and Emerging Low Precision Operators in HPC Application
Eric Petit (Intel), Jack Dongarra (University of Tennessee), Marc Casas (Barcelona Supercomputing Center), Peter Dueben (ECMWF)

With ever-increasing need for computation of scientific applications, major energy constraints, and new application domains such as machine learning, general purpose processor arithmetic is entering a new burst of evolution. Novel hardware and software solutions are explored to leverage emerging low precision operators. Indeed, a better fit in precision usage can provide higher flops, higher energy efficiency, lower communication bandwidth and volume needs. To fully exploit this potential optimization, all the application design ecosystem needs profound evolution with new numerical algorithms, low and mixed precision libraries, and dedicated tools for validating, optimizing, and debugging precision issues. This BoF session will present four technical contributions to this topic on different aspects: AI, linear algebra libraries, tools, and applications. This presentation will be followed by an interactive round-table with the speakers.

Room: Substanz 1, 2
1:45 pm - 2:45 pm

Defining HDF5 Future

Defining HDF5 Future
Elena Pourmal (The HDF Group), Steven Varga (The HDF Group), Gerd Heber (The HDF Group), Kesheng Wu (LBL), Lukas Szajkowski (WizzDev), Gerd Heber (The HDF Group)

HDF5 is a unique, open-source, high-performance technology suite that consists of an abstract data model, library, and file format used for storing and managing extremely large and/or complex data collections. The technology is used worldwide by government, industry, and academia in a wide range of science, engineering, and business disciplines.

We will provide a forum for the HDF5 user community to share ideas, present problems, outline possible solutions and discuss future direction of HDF5 and the HDF5 ecosystem. Elena Pourmal will present HDF5 features under development, the HDF5 roadmap, including upcoming releases and launch a discussion for HDF5 roadmap and community involvement in HDF5 development. Elena's presentation and discussion will be followed by a discussion led by Steven Varga who is an active member and contributor of the HDF community. He will answer questions from the audience and survey the latest developments and challenges in the HDF5 ecosystem including (but not limited to): ● Storage devices and platforms for HDF5 (cloud, object stores, HDFS, PFS), VFDs and VOLs ● HDF5 language bindings (C++/LLVM, Python, Julia, R) ● HDF5 library development and community code contributions to HDF5 ● HDF5 Performance and productivity (benchmarks, profiling, Tau plugin) ● I/O concurrency (multithreading, MPI-I/O) ● Sparse data and HDF5 ● HDF5 connectors for Apache Spark and Drill ● HDF5 tools, including third-party tools and vendor support Steven and Elena will encourage HDF5 community members to share their experiences and challenges with HDF5. The summary of discussion will be shared with the HDF5 community.

Room: Kontrast
1:45 pm - 2:45 pm

XALT and Related Technologies: Job-Level Usage Data on Today's Supercomputers

XALT and Related Technologies: Job-Level Usage Data on Today's Supercomputers
Robert T. McLay (University of Texas at Austin, UT Austin)

We're interested in what users are actually doing: everything from which applications, libraries, and individual functions are in demand, to preventing the problems that get in the way of successful computational research. And this year we're especially interested in some of the next great challenges, including (1) understanding the needs of formerly non-traditional research communities that comprise half the user community and whose non-MPI workflows consume more than a third of the computing cycles;

(2) putting usage data in the hands of end users interested in records of their own job-level activity to facilitate, for example, reproducible research. We are now tracking individual Python packages and similar usage within other frameworks like R and MATLAB.

XALT (xalt.readthedocs.org) is a battle-tested tool focused on job-level usage data; it enjoys a well-documented history of helping administrators, support staff, and decision makers manage and improve their operations. The small but growing list of centers that run XALT includes NCSA, UK NCC, KAUST, NICS, the University of Utah, and TACC. Join us a far-ranging discussion that will begin with an overview of new XALT capabilities before it ventures into broader strategic and technical issues related to job-level activity tracking.

Room: Analog 1, 2
2:45 pm - 3:45 pm

The Message Passing Interface: Towards MPI 4.0 and Beyond

The Message Passing Interface: Towards MPI 4.0 and Beyond
Martin Schulz (Technical University of Munich, Chair of Computer Architecture and Parallel Systems)

The Message Passing Interface (MPI) is one of the most dominant programming models for HPC environments. Its specification is driven by the MPI forum, an open forum consisting of MPI developers, vendors and users. This BoF Meeting will provide some insight into the current topics discussed in the forum as well as the process of how features are added to the standard. It is intended to keep the larger HPC community informed about current activities and long-term directions, as well as encourage larger community participation in this crucial standard for the Supercomputing community.

The work in the forum currently targets MPI 4.0, tentatively scheduled for 2020, as well as long term topics beyond that, which include support for fault tolerance in MPI, improved support for hybrid programming models, addition of persistent versions of collective routines, exploration of a sessions concept MPI to improve scalable runtime support and the addition of new tool interfaces.

This BoF Meeting continues the tradition of MPI Forum BoFs held in the last years, which have been well attended and widely successful. The session will be led by Martin Schulz, the current chair of the MPI forum with the help of leading experts on MPI who are active in the MPI forum. The exact list of speakers will be determined closer to ISC 2019 based on current topics in the MPI forum. Previous sessions featured speakers included William Gropp, Pavan Balaji, Torsten Hoefler or Dan Holmes.

Room: Konstant
2:45 pm - 3:45 pm

Personalised Medicine and the HPC Industry

Personalised Medicine and the HPC Industry
Peter Coveney (University College London), Marco Verdicchio (Surfsara), Gavin Pringle (Edinburgh Parallel Computing Centre (EPCC)), Cristin Merritt (Alces Flight Limited), Cyril Mazauric (Atos), Marcin Ostasz (BSC, ETP4HPC)

How to bring HPC to medical SMEs, clinical researchers and hospitals? As we are nearing the exascale era, too few benefits from such computational power, and even fewer achieve excellence in HPC application delivery and use. By bringing together the biomedicine community and the HPC industry, we hope to help the community better embrace upcoming technologies, and help the industry better understand the needs: fault tolerance, data and compute resources, access mechanism (such as urgent computing, on-demand computing, advanced reservation…), computing power, code efficiency. Which feature is critical for biomedicine? Is Industry aware of it, and what answers are planned in the future? Overall, how to bring these improvements to the people who diagnose, to the drug discoverer, or even to your doctor? As a Centre of Excellence working towards the advancement of computationally based modelling and simulation within biomedicine using large-scale and cloud computing resources, CompBioMed is a significant contributor to this debate, with experience to share, especially through its three exemplar research areas: cardiovascular, molecularly-based and neuro-musculoskeletal medicine. To complete the picture, we hope industry stakeholders will share their vision of a complex area involving so many different areas of expertise. To feed the debate, all interested parties are welcome to attend and help paving the way to excellence.

Room: Substanz 1, 2
2:45 pm - 3:45 pm

What are the Greatest Challenges to be Addressed by Academic HPC Systems Research?

What are the Greatest Challenges to be Addressed by Academic HPC Systems Research?
Paul Carpenter (BSC), Theo Ungerer (University of Augsburg), François Bodin (University of Rennes I), Dietmar Fey (Friedrich-Alexander-University (FAU)), Avi Mendelson (Technion, Nanyang Technical University)

Radical changes are foreseen in all aspects of high-performance computing systems over the next decade. The end of CMOS scaling is bringing new and emerging technologies (quantum, neuromorphic, etc.) and heterogeneous accelerators (GPUs, FPGAs, TPUs, etc.). Meanwhile, HPC applications are being complemented by machine learning and extreme data, and are evolving to model problems more difficult than previously thought possible. In this context, we need a thriving, high-quality and relevant European community in academic HPC systems research. This session will bring together academic researchers and interested stakeholders to discuss, assess and contribute to Eurolab4HPC's vision for academic research in high performance computing. Four expert presenters will engage with the audience in a lively and hopefully controversial interactive session.

Eurolab4HPC is a two-year H2020-funded project with the bold commitment to make Europe excel in academic research and innovation in HPC technology. Eurolab4HPC has the overall goal to strengthen academic research excellence and innovation in HPC in Europe, by structuring the HPC community, disseminating community news, promoting entrepreneurship, and stimulating technology transfer.

Eurolab4HPC published the first version of its Eurolab4HPC Long Term Vision on High-Performance Computing in August 2017. This document targeted the period 2023–2030, over which it predicted major changes across high-performance computing. It surveyed the landscape of HPC systems research, driven by a push from emerging technologies and a pull from new and evolutionary applications. This session is intended to be the first public workshop in the process of preparing the 2020 update, which will be published in January 2020.

Room: Kontrast
2:45 pm - 3:45 pm

100% Open Source Full Stack Cluster Management

100% Open Source Full Stack Cluster Management
Roland Fehrenbacher (Q-Leap Networks GmbH), Ansgar Esztermann (Max-Planck-Institute for Biophysical Chemistry)

Setting up and operating HPC clusters remains a challenge. Individual software packages are freely available for most functionality, however an integrated open-source solution covering all aspects of cluster management was missing until recently.

Qlustar's mission is to fill this gap: As a mature Cluster OS it includes a scalable boot/image technology coupled with a powerful management software that allows precise configuration of cluster components as well as their efficient operation. Its ease of use frees valuable human resources making them available to

improve scientific research done with HPC instead.

The decision to fully open-source Qlustar about one-year ago generated substantial momentum with more than 80 new world-wide installations. This indicates that the possibility to standardize on a free but supported vendor-neutral cluster software stack is an attractive option for organizations.

This session will have two presentations, where the first one will briefly outline the present features of Qlustar and the second will be about about the motivation and steps taken so far in the direction towards open-source standardization of HPC management software at the Max-Planck-Institute for Biophysical Chemistry.

The goal of this BoF is to bring together developers, HPC cluster admins and hardware vendors to identify the most pressing issues to further enhance Qlustar's suitability as an open-source full stack HPC management solution. 50% of the time will be dedicated to Q&A sessions after the two presentations and a concluding extended survey concerning future requirements for Qlustar from the sysadmin and/or hardware vendor side based on feedback from the audience.

Room: Konstant
3:45 pm - 4:45 pm

LLVM in HPC - Where we are and Where we Need to be

LLVM in HPC - Where we are and Where we Need to be
Anja Gerbes (Center for Scientific Computing), Johannes Rudolf Dörfert (Argonne National Laboratory), Simon Moll (Saarland University), Joel Denny (Oak Ridge National Laboratory), Sameer Shende (University of Oregon), Will Lovett (Arm)

In the HPC community compilers allow the coder to make use of tools to increase better performance and capability. In this space, especially LLVM has been gaining attention during the last years. LLVM evolved to be the universal backend not only for C/C++ but also for new languages like Julia and Rust. As a compiler framework, it is designed to support program analysis and transformation for arbitrary programs at compile-time, link-time, and run-time. The key to success is its performance and adaptability, both of which derive from its unique design and implementation.

In this BoF, participants from academia and science discuss the current status of LLVM in HPC and how it can best be improved to benefit a broader community. We plan to have LLVM developers additionally highlight existing and emerging features interesting for scientific software and HPC applications. We invite anyone experienced or simply interested in the LLVM compiler framework, or any of its subprojects,

to participate in the discussion as a stepping stone to get involved.

Room: Substanz 1, 2
3:45 pm - 4:45 pm

Performance Portability and Productivity: Panel Discussion

Performance Portability and Productivity: Panel Discussion
Brandon Cook (LBNL), Thorsten Kurth (LBNL), Robert Hoekstra (Sandia National Laboratory), Ana Varbanescu (University of Amsterdam), Guillaume Colin Verdière (Commissariat à l'Energie Atomique), Didem Unat (Koç Üniversitesi), Simon McIntosh-Smith (University of Bristol), Gihan Mudalige (University of Warwick)

The ability for applications to achieve both portability and high performance across computer architectures remains an open challenge. It is often unrealistic or undesirable for developers to maintain separate implementations for each target architecture, yet in many cases, achieving high performance and fully utilizing an architecture's underlying features requires the use of specialized language constructs and libraries. Likewise, abstractions and standards that promise portability cannot necessarily deliver high performance without additional algorithmic considerations, and performance compromises are often made to remain portable. Application developers, who strive to work productively while balancing these concerns, often find the goal to be elusive.

There is a clear need to develop ways of managing the complexity that arises from system diversity that balance the need for performant specializations with the economy of appropriate and efficient abstractions. Despite growth in the number of available architectures, there are similarities that represent general trends in current and emerging HPC hardware: increased thread parallelism; wider vector units; and deep, complex, memory hierarchies. This in turn offers some hope for common programming techniques and language support as community experience matures.

In this BoF a panel of experts will draw on expertise in application development, programming model research and computer architecture in an open conversation to discuss and share ideas, practical experiences, and methodologies for tackling the challenge of achieving performance portability and developer productivity across current and future homogeneous and heterogeneous computer architectures.

Room: Kontrast
3:45 pm - 4:45 pm

Omni-Path User Group (OPUG) Meeting

Omni-Path User Group (OPUG) Meeting
David Benoit (University of Hull), Daniela Galetti (Cineca), Philip Murphy (Intel), Dhabaleswar Panda (The Ohio State University)

Following on from a successful BoF at ISC18, the proposed event will continue to provide a forum for users and other interested parties to exchange their experience and insights using Intel's Omni-Path Architecture (OPA) communication fabric. Indeed, OPA is now used as production fabric in a growing number of Tier-0 HPC sites (Marconi, MareNostrum, to name a few). However, Omni-Path remains a relatively "young" fabric and thus sharing performance results, issues and/or recommended future OPA developments is valuable to the growing community of OPA adopters. This Bof will contain an introduction, Intel OPA update, short panel presentations/user cases from experienced OPA users and group discussion. We plan to explore themes related to uses of OPA on containerised systems, performance improvements and comparison with more established fabrics.

Break

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Sunday, June 16th

Room: Analog 1, Analog 2, Applaus, Substanz 1, Substanz 2, Kolleg, Konstant
8:00 am - 9:00 am

Welcome Coffee

Room: Effekt, Expose, Extrakt
8:00 am - 9:00 am

Welcome Coffee

Room: Areal
11:00 am - 11:30 am

Coffee Break

Room: Areal
1:00 pm - 2:00 pm

Lunch

Room: Mövenpick Foyer
1:00 pm - 2:00 pm

Lunch

Room: Areal
4:00 pm - 4:30 pm

Coffee Break

Monday, June 17th

Room: Areal
7:30 am - 9:00 am

Welcome Breakfast

Room: Panorama Foyer, Panorama 2, Panorama 3
10:30 am - 11:00 am

Coffee Break

Room: Areal
11:45 am - 1:00 pm

Lunch

Room: Exhibition Hall
3:00 pm - 4:00 pm

Coffee Break

Tuesday, June 18th

Room: Foyer Hall 3
7:30 am - 10:00 am

Welcome Coffee

Room: Exhibition Hall, Areal
10:00 am - 11:00 am

Coffee Break

Room: Exhibition Hall
12:30 pm - 1:45 pm

Lunch

Room: Panorama Foyer
3:15 pm - 3:45 pm

Coffee Break

Room: Exhibition Hall
3:15 pm - 3:45 pm

Coffee Break

Room: Panorama Foyer
4:45 pm - 5:15 pm

Coffee Break

Room: Exhibition Hall
4:45 pm - 5:15 pm

Coffee Break

Wednesday, June 19th

Room: Foyer Hall 3
7:30 am - 10:00 am

Welcome Coffee

Room: Exhibition Hall, Areal
10:00 am - 11:00 am

Coffee Break

Room: Exhibition Hall
12:30 pm - 1:45 pm

Lunch

Room: Panorama Foyer
3:15 pm - 4:00 pm

Coffee Break

Room: Exhibition Hall
3:15 pm - 4:00 pm

Coffee Break

Room: Exhibition Hall
4:45 pm - 5:15 pm

Coffee Break

Room: Panorama Foyer
5:00 pm - 5:30 pm

Coffee Break

Thursday, June 20th

Room: Foyers
8:30 am - 9:00 am

Welcome Coffee

Room: Foyers
11:00 am - 11:30 am

Coffee Break

Room: Platinum 1, Platinum Foyer
1:00 pm - 2:00 pm

Lunch

Room: Foyers
4:00 pm - 4:30 pm

Coffee Break

Distinguished Speaker

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Monday, June 17th

Room: Panorama 2
5:00 pm - 6:00 pm

Distinguished Speakers

Exascale Computing in China: Major Issues and Status
Depei Qian (Sun Yat-sen University, Beihang University)

Starting with a brief historical review on high performance computing in China, this talk presents the current efforts of China's national key project on exascale computing. After discussing the technical challenges, the talk proposes some major research issues on exascale computing. The current research activities carried out by the key R&D project are then summarized and presented, including the efforts on exascale prototypes, exascale application software and software development support, and high performance computing environment enabling the effective use of the exascale computers. Perspectives and some open issues are raised towards the end of this talk.

Machine Learning and HPC for Cancer Biology
Frederick Streitz (Lawrence Livermore National Laboratory)

Room: Panorama 3
5:00 pm - 6:00 pm

Distinguished Speakers

Applied Ethics in Artificial Intelligence and Deep Learning
Simon Hegelich (TUM - Bavarian School of Public Policy)

There is an ongoing debate about ethical artificial intelligence. Unfortunately, parts of this debate do not address the technical dimensions of state of the art methods, especially deep learning. From an interdisciplinary perspective there are three main challenges for ethical deep learning: hidden bias, confusion of causality and correlation, and black-box algorithms. These challenges have to be addressed by technical solutions and sound social science analysis.

Machine Learning – Where are we at? Where are we headed?
Christian Bauckhage (Fraunhofer-Institut für Intelligente Analyse- und Informationssysteme IAIS)

Big Data and High Performance Computing are two of the major drivers behind recent progress in machine learning and artificial intelligence. In this presentation, we first review the current state of the art in in data-driven statistical learning and point out some of the limitations of the currently most popular methods. Then, in an attempt to predict future developments in this arena, we look at quantum computing and its potential benefits for common machine learning problems.

Wednesday, June 19th

Room: Panorama 2
4:00 pm - 5:00 pm

Distinguished Speakers

The Economics of Computing at the End of Moore's Law
Neil Thompson (MIT – Computer Science and Artificial Intelligence Lab, Harvard – Lab for Innovation Science)

The success of Moore's Law came not just from enormous technical improvements, but from a virtuous economic cycle that funded innovation and brought users onto a common platform. This paper argues that technological and economic forces are now pushing computing in the opposite direction, making computer processors more specialized and semiconductor manufacturers less able to amortize costs. This process has already begun, driven by the slowdown in Moore's Law and the success of parallelizable algorithms such as Deep Learning. This trend towards specialization threatens to fragment computing into 'fast lane' applications that get powerful customized chips and 'slow lane' applications that get stuck using general purpose chips whose progress fades.

The Quantum Flagship: Quantum Technologies - From Basic Science to Applications

Kristel Michielsen (Jülich Supercomputing Centre (JSC), RWTH Aachen University)

After the Graphene Flagship and the Human Brain Project, the Quantum Flagship is the third long-term and large-scale research and innovation initiative of this kind funded by the European Commission. The main goal of the Quantum Flagship is to transfer quantum physics research from the lab to the market by means of commercial applications. The Quantum Flagship has started in October 2018 with 20 projects in which researchers from academia and industry are involved. These projects cover research and technology development in the areas of quantum computing, quantum simulation, quantum communication, and quantum sensing and metrology.

Exhibition

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Monday, June 17th

Room: Exhibition Hall
3:00 pm - 8:30 pm

Exhibition

Tuesday, June 18th

Room: Exhibition Hall
10:00 am - 6:00 pm

Exhibition

Wednesday, June 19th

Room: Exhibition Hall
10:00 am - 6:00 pm

Exhibition

Exhibitor Forum

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Monday, June 17th

Room: Booth N-210
3:20 pm - 6:20 pm

Exhibitor Forum

RNT Rausch GmbH: Information will follow soon

Atempo: Dirac - OCF – Atempo, a Winning Trio for the Successful Implementation of a Multi-Petabyte Archiving Project
Alastair Basden (Durham University)

An HPC storage system needs to rapidly process large volumes of data yet many challenges threaten petabyte-scale storage, backup and archiving. Large NAS, Lustre or GPFS file systems require powerful and reliable solutions to continue to protect these massive unstructured data sets. But what should companies look for when selecting vendor-agnostic backup/restore solutions for these petabyte scale environments? Dr. Basden will share his view and recommendations on how to successfully implement a petabyte-scale archiving project with an economical solution.

Arm: Arm in HPC
Brent Gorda (Arm)

“Arm in HPC” will provide an update on Arm’s activities and plans in support of the HPC segment, including CPU architecture, SoC design IP, and software ecosystem. Furthermore it will highlight the various engagements and collaboration projects underway between Arm, its partners, and strategic end-users.

AMD: Silicon and Software Solutions for HPC
Andy Parma (AMD)

Momentum is building for AMD's HPC business, with a growing number of customers announcing deployments using the AMD EPYC™ 7000 Series Processor. Come learn about the latest updates to the AMD EPYC™ Server Processor product line and AMD Software for HPC.

Automation N.V: Design and Operation of a 3 MW Data Center Based on Modular Containers
Rainer Schwemmer (CERN)

CERN, in cooperation with LHCb, is currently building a new 3MW data center. The purpose of this data center is the consolidation and filtering, in real time, of a 5 TB/s data stream coming from a High Energy Physics experiment. The data center is divided into 2 logical units. Unit 1, consisting of two 18m container modules, receives the data stream on approximately 17000 optical links and assembles and distributes data sets to the filter processing unit. Unit 2 consists of four 18m container modules housing the bulk of the computation power which is used to reduce the immense data volume to more manageable quantities. The data center modules themselves are cooled via indirect fresh air cooling with an additional adiabatic cooling stage during warm periods. Rack power density is 22 kw per rack. At the time of this presentation we will have been operating the first stage of this data center for nearly 6 months and will present first results and lessons learned from its construction and operation.

National Supercomputer Center in Guangzhou: The Deep Learning of Biomedical Big Data on Tianhe-2
Yuedong Yang (National Supercomputer Center in Guangzhou)

With the revolutionary development of the next generation sequencing techniques, the amount of biological sequence data is exponentially exploding that was estimated to arrive in the ZB level within 10 years. As the biological data is of high dimension, high noise, but relatively small samples, it is challenging to directly learn from the big data. Fortunately, many efforts have been made to study molecular mechanisms underlying in life, and the accumulated knowledge provides a reliable way for efficient mining of the biomedical big data. At the same time, the learning of the big data can rapidly expand the available knowledge over the life science. Based on the "Tianhe-2" supercomputer, we have employed deep learning techniques (CNN, RNN, and the combinations) to develop a series of bioinformatics algorithms for accurate prediction of protein structure, functions, and interactions. These accurate predictions were further integrated to analyze noisy sequencing data for biological applications, including annotations of disease-causing mutations, cancer prognosis, and drug discovery and repositioning. Moreover, we are developing a biomedical cloud platform integrated with biomedical database and bioinformatics tools for data analysis and predictions. Such platform will provide a one-stop site for both biological and medical applications.

Beijing BEILONG Super Cloud Computing co., Ltd: Speedup your Research by Supercomputing Cloud of CSTCloud

Jian Chen (Beijing BEILONG Super Cloud Computing co., Ltd)

As part of the China Science and Technology Cloud(CSTCloud), Supercomputing Cloud is a unified platform of China's supercomputing resources, which aggregates multiple National Super Computer Centers and commercial computing resources. Upon the computing infrastructure, we also supply a 7*24 technology support for the user's job. The scientists will speedup their research work by what we do.

Fraunhofer-Institute for Algorithms and Scientific Computing (SCAI): StandICT.eu: Supporting European Experts in International Standardisation of Cloud, IoT, Cyber Security, Big Data, 5G and AI

Wolfgang Ziegler (Fraunhofer-Institute for Algorithms and Scientific Computing (SCAI))

The talk presents the European StandICT.eu project which aims at leveraging European contributions to standardisation in the five priority domains Cloud, IoT, Big Data, 5G, Cybersecurity and Artificial Intelligence. We'll present the funding approach of Standict.eu with a focus on the funded activities in the field of cybersecurity, the results achieved until now, the funding opportunities until the end of the project and future perspectives. Additionally, we will also present Standards Watch, a sustainable observatory for standards, standards developments and related information maintained by StandICT.eu. The third focus of the presentation is on our study of the current AI standardisation landscape.

Univa

Fritz Ferstl (Univa)

It has become critical for many organizations to find high-performance computing (HPC) solutions that can scale with their compute-intensive workloads as a way to gain a competitive advantage. This drive for virtually unlimited HPC capacity and extreme-scale, whether it be on-premise, in the cloud or in a hybrid environment, makes sense given the right environment. Yet organizations are looking for ways to speed up innovation by having greater flexibility, predictability and scale as their HPC requirements grow and evolve.

Western Digital, a leader in data-centric solutions, alongside AWS and Univa, sought to achieve extreme-scale within its data center as a way to build a cloud-scale HPC cluster on AWS to simulate key elements of upcoming designs for their next-generation hard disk drives (HDD). The three companies worked together to evaluate the impact of running electro-magnetic engineering simulations on a massive HPC cluster built on AWS using Amazon EC2 Spot Instances, with the goal of completing the project in the

smallest amount of time and at the lowest cost. As a result, Western Digital ran approximately 2.5 million simulation tasks on a Spot-based cluster of over one million vCPUs to determine optimal device characteristics that would help improve product quality, performance, reliability and durability for next-generation HDDs. The collaborative effort achieved a key milestone by completing what was initially a 480-hour (20-day) project in just 8 hours. This presentation will discuss how Western Digital was able to work with Univa and AWS to achieve extreme-scale HPC to achieve a competitive edge.

Tuesday, June 18th

Room: Booth N-210
10:40 am - 5:20 pm

Exhibitor Forum

Supermicro: High Performance Green Computing
Martin Galle (Supermicro, Super Micro Computer B.V.)

IT managers are increasingly seeking out suppliers of high performance, cost-effective and energy-efficient Green IT products. Their primary objective is to reduce skyrocketing data center operational costs, a large proportion of which are energy-related costs. As these energy costs continue to escalate, users will need to spend significantly more to power and cool their server hardware than they require to purchase it.

Supermicro's Resource-Saving Architecture continues our tradition of leading the market with Green IT innovation that helps the environment as well as provides Total Cost of Ownership (TCO) savings for our customers while reducing the Total Cost to the Environment (TCE).

Mellanox Technologies: Super-Connecting the World's Number One Supercomputers
Scot Schultz (Mellanox Technologies)

Mellanox continues our leadership as the best interconnect worldwide for HPC and AI. The latest intelligent interconnect devices, such as Mellanox Quantum HDR 200Gb/s and ConnectX-6 are enabling the next generation of in-network co-processing, and a more effective mapping of communication between devices in the system which increases system performance by an order of magnitude. Similar to the ecosystem for HPC, we will outline why every major framework for machine learning now natively supports Mellanox acceleration capabilities to achieve world-record setting performance. By providing the best-in-class network and acceleration engines for HPC and Artificial Intelligence which already

employed by the top systems in the world, including Canada, China, Japan and the US, we will explore the next generation capabilities of these smart-interconnect devices to achieve the next milestones towards Exascale and extreme distributed machine learning system.

Oracle: Running HPC Workloads on the Cloud for a Fraction of the Cost but Market Leading Performance!

Taylor Newill (Oracle Cloud Infrastructure)

Running specialized workloads has generally either been very expensive or not as performant in the public cloud space, getting a best performance and best pricing has been a challenge as these workloads require every ounce of performance and are generally mission critical workloads. With Oracle working on Exadata over the last decade, we've used that heritage to design and build the next generation of HPC capabilities in the cloud allowing for extreme flexibility with on-premise levels of performance. You no longer have to compromise. Learn how you can get started with demos, best practices and how we can lift and shift these workloads into the cloud with minimum effort. We'll share technical walkthroughs and detailed architectures in the session along with a view into the portfolio of offerings.

Amazon Web Services: HPC on AWS: Every Workload Accepted

Ian Colle (Amazon Web Services)

In this session, Ian will talk about the new AWS services that now make it possible to run any type of HPC workload in the cloud - at scale. Two services of particular importance that Ian will talk about include the Elastic Fabric Adapter - a new low-latency network interface to scale tightly-coupled HPC workloads to thousands of cores, and Amazon FSx for Lustre - a high-performance file system optimized for fast processing of workloads such as machine learning and High Performance Computing. Finally, Ian will talk about the opportunity to accelerate the pace of innovation by combining HPC workflows with new technologies like Artificial Intelligence (AI) and Machine Learning (ML).

CoolIT Systems

Jason Zeiler (CoolIT Systems)

CoolIT Systems' Rack DCLC platform is a modular, rack-based liquid cooling solution that delivers dramatic increases in rack densities, component performance and energy efficiencies. This passive technology can be deployed with any server in any rack, making it a truly flexible solution that creates a TCO edge in today's highly competitive marketplace. Discover how direct liquid cooling can be deployed in your datacenter and what important steps must be considered when planning begins.

Verne Global: Analysing the Evolution from Classic HPC to New HPC
Bob Fletcher (Verne Global)

This presentation will look at the evolution of classic HPC - typically the domain of government, education and research centers and the "Top-500", and new HPC - advanced computing built for AI and machine learning that's as agile as it is powerful, cloud native, often containerised and fully GPU supported.

We will draw on case studies based at our Icelandic campus to demonstrate the transition we're seeing.

DDN Storage: Announcing EXA5 – A profound transformation of HPC and AI storage: Accelerated innovation AND continuous availability, robust user and data management with blistering parallel performance.
James Coomer (DDN Storage)

Organizations are increasingly looking for easy to use, robust, and highly scalable data management solutions, which can be flexibly deployed in multi-cloud environments, and will deliver faster insight while maximizing the value of their complex, distributed data. Emerging workflows in AI, Deep Learning, Analytics as well as HPC are continuing to push I/O infrastructures and creating complexity because of the diversity of data.

DDN is excited to announce the availability of EXAScaler5, a dramatic leap forward in solving complexity for customers that are struggling to manage data from edge to core, and over various architectures from flash to hybrid and multi-cloud. Come hear Dr. James Coomer, senior vice president of products for DDN, discuss this newest release, and what else DDN has planned to address evolving communications networks like 5G, data management for IoT, and how storage will evolve to address Big Data, streaming and mixed workloads efficiently at scale.

Red Hat: Enabling Infrastructure Automation with Red Hat
Brian Tannous (Red Hat)

In this session you will learn about how Red Hat provides distributed systems, storage, and tooling to provide you with robust infrastructure and development automation. We will focus on distributed computing through Red Hat OpenShift, a leader in Enterprise Kubernetes, as well as Red Hat Storage solutions. You will see high performance computing in action with GPU assisted workflows, and understand the latest operator centric cluster methodologies in action.

Panasas, Inc.: High Performance for all Data Types – The Next-Generation Object Storage Device in a Portable Parallel File System

Curtis Anderson (Panasas, Inc.)

Delivering consistently high performance regardless of data type and complexity is essential for supporting traditional and emerging HPC applications. This talk will describe the performance and data management capabilities of a parallel file system with an object backend by highlighting the internal architecture of the new ActiveStor® Ultra Object Storage Device (“OSD”) within the portable PanFS parallel file system. We will share the latest performance results, examine software and hardware architecture details, and show how the application of intelligent data and metadata management enables the processing of large and complex data sets without performance limitations.

Presentation highlights include:

• Designing a highly portable OSD software stack that features modern design patterns and the highest performance, while retaining high reliability and ease-of-use

• Separating file system metadata into a software database on a low-latency NVMe SSD

• Integrating the OSD into commodity hardware platform designs that include a full performance range of storage devices: NVDIMM(s), NVMe SSD(s), SATA SSD(s), and SATA HDD(s)

Hewlett Packard Enterprise: How HPE Delivers Leading Edge Technology for all HPC and AI Users
Ben Bennett (Hewlett Packard Enterprise)

HPE’s commitment to R&D constantly creates new technologies. We work with select HPC users across the world on collaborative research products using these technologies. This helps HPE define leading edge HPC products which are robustly productized to allow computation at scale, advanced AI & deep learning, and data intensive computing. We then package products with the most comprehensive HPC portfolio of software, storage, fabric, supported by HPE Pointnext services (advisory and consultative) and lab testing/validation. HPE successfully delivers best of breed solutions delivered on-premises or Hybrid HPC.

Huawei: Huawei Intelligent Computing Supercharges HPC and AI
Yihui Xiong (Huawei Technologies Co.,Ltd.)

Huawei drives innovation across chips and system architecture, and builds diversified computing platforms to meet HPC requirements, as well as accelerating the integration of AI and HPC. Huawei leverages deep co-innovation and optimization capabilities with HPC industry applications and smooth collaboration with Huawei Cloud, working alongside customers to embrace the transformative power of future HPC.

Intel: From Data to Insight with AI
Stephan Gillich (Intel)

Simulation - commonly seen as “HPC” is an area which has overlap with AI: Can you use AI methods to improve simulation? How can you run AI applications on HPC Systems? We will give an overview of respective technology for AI, including HW platforms & SW stacks to enable successful development of AI solutions.

Atos: Autonomous Driving: HPC Under the Hood?
Cédric Bourrasset (Atos)

Producing Level 5 Autonomous driving vehicles will require a safe decision-making system able to take into account a large uncertainty set coming from sensors (cameras, lidar, …) and car surroundings, including weather condition, traffic, pedestrian behavior… Such a decision system needs to be thoroughly simulated before launching on-road tests where wrong decisions could have a direct impact on human lives.

Atos, as a key European player in the HPC market, with the support of its partners, can help the autonomous vehicles simulation market to address the whole pipeline needed for developing the next generation of autonomous vehicles. This presentation will tackle all the challenges encountered in the Level 5 simulation field, from on-car data collection to datalake solution and data management governance, including large scale HPC systems integrating a mix of HPC and AI workflow management tools. It will also address the development of the European Processor Initiative (EPI) aiming to deliver the first European processor integrating a core architecture designed both for HPC simulation needs and for the embedded automotive market.

Dawning Information Industry Co., Ltd.: New Generation of Silicon Cube Supercomputer
QING JI (Dawning Information Industry Co., Ltd.)

This new generation of Silicon Cube series High Performance Computer adopted the phase-change liquid cooling technology with the highest computing density and energy efficiency. Meanwhile, the system applied many other crucial technologies to make it a world leading HPC solution in terms of technology and engineering implementation, including computing, networking, storage, cooling, overall management and so on. The product meets for the higher demands of compute density, energy efficiency, and storage. In general, the highlights of the new HPC series lay on the comprehensive improvements in PUE, network optimization and scalability. Comparing with its predecessor launched in 2015, the new series delivers a highly technical and successful result in solving power consumption,

extendibility and reliability challenges.

Kingston Technology: HPC Enabler - The Performance Behind the Machine
Adrien Viaud (Kingston Technology)

tba

Lenovo: Lenovo AI for Good
Valerio Rizzo (Lenovo)

Data are not good data just because of their size, so big data per se are not a value. The added value is actually present and perceivable only if simple, comprehensible and possibly new and actionable information can be extracted from the big mass of data with a reasonable effort.

The massive speed of data growth and variety, are challenging human cognitive capacity. Educated guessing as the process of inference when information is not at hand was quite the norm in the past; today the bottleneck of human ability to process information can be bypassed if data are correctly integrated to produce new actionable knowledge, thus augmenting human cognitive capacity.

AI and machine learning represent a fundamental shift in how data is interpreted. The more data you feed AI models, the more intelligent they become.

By connecting commercial partners with our in-house AI experts and expertise at leading Universities and providing state of art hardware infrastructure, Lenovo is helping solve the toughest challenges facing humanity

Altair: How We Get to the Future: HPC & AI
Bill Nitzberg (Altair)

At the heart of ‘what is HPC?’ and ‘what is AI?’ is a common pursuit: taking today’s technology and pushing it further, to the boundary of what is possible. In fact, if something can be done easily today, it’s not considered HPC, and it’s not AI. It’s just engineering. The future is bringing these two pursuits together, using each to advance the other: scaling up AI calculations by integrating tightly with HPC technologies, and making HPC more efficient and effective by leveraging AI techniques. The future of computing combines HPC and AI for Exascale, for Cloud, and for Green Computing.

Quanta Cloud Technology (QCT): Enabling Your Performance, Enabling Your Business

Maurizio Riva (Quanta Cloud Technology (QCT))

QCT offers complete spectrum of optimized platforms from edge computing, central office to data centers. We had a huge progress powering cloud service providers with our server, storage, network switch and rack systems. Now, we're seeing all the latest trend such as autonomous car, smart healthcare, which are integrating intelligence. Our goal is to provide an end-to-end infrastructure platform, all the way from edge computing to data centers. There are four pillars that we've been investing and incubating our capabilities and offerings, including AI, 5G, software define infrastructure and as well as the disaggregate hardware and software. We have deep and long-term collaborations with Intel, Nvidia and our ecosystems partners by integrating the pioneering technologies for our customers at an early stage.

Bright Computing: Edge to Core to Cloud – Making the Vision a Reality
Martijn de Vries (Bright Computing)

In this session, Martijn de Vries, CTO at Bright Computing will look at the evolution of HPC and the emerging requirement for infrastructure to span the edge, the core, and the cloud. Martijn will explore the role that cloud computing has played in revolutionizing the way that organizations store and use their data, and the associated limitations, such as latency, bandwidth, and security that necessitate edge computing alternatives. Martijn will address the challenges of building and managing a distributed infrastructure that includes edge and cloud; and explain how organizations can achieve their goal of running a shared infrastructure that spans the edge, the core, and the cloud.

SUSE: Enabling New Discoveries with SUSE Linux Enterprise for HPC
Jeff Reser (SUSE), Jay Kruemcke (SUSE)

SUSE offers a highly scalable, high performance open source computing system that enables users to harness the power of the supercomputer for day-to-day business. SUSE accelerates innovation with new solutions developed and delivered with a strong ecosystem of partners. We will discuss the latest exciting initiatives within this ecosystem which improve scalability and performance, realize faster time to value and answer the needs of future HPC systems.

Wednesday, June 19th

Room: Booth N-210
10:20 am - 5:00 pm

Exhibitor Forum

NetApp: Enterprise Adoption of AI/ML Techniques Drive HPC Infrastructures
Stan Skelton (NetApp)

High Performance Computing workloads are typically built using a scale-out parallel architecture. At the heart of these infrastructures are Parallel File Systems. Examples include BeeGFS (ThinkParQ), SpectrumScale (IBM), Lustre (DDN) and StoreNext (Quantum). HPC and associated sub-markets have led the adoption of AI/ML techniques well ahead of traditional IT and Enterprises. As AI/ML techniques are adopted in the Enterprise we see deployment of Parallel File Systems and supporting system architectures. This talk will address how some HPC infrastructures will be challenged to supply the appropriate Enterprise requirements of Data Integrity, high reliability and security. We will also illustrate how some HPC infrastructures have made the step to fill the gaps required for Enterprise Data Centers as they adopt AI/ML techniques. We will also review new industry initiatives that support the system and architectural changes needed for AI/ML such as Gen-Z, SNIA Persistent Memory Initiative and SNIA Computational Storage.

NEC Deutschland GmbH: Vector Computing in the Year 2019
Michael Wirth (NEC Deutschland GmbH)

Vector Computers have dominated the high end HPC market from the 1980's. By the end of the century, most supercomputers used scalar processors, and clusters became more and more popular, mainly due to their comparably low cost. Yet, vector processors have significant advantages on a large number of applications, therefore NEC continue to develop and produce modern vector processors. This talk gives an overview of modern day vector computing, from single-node acceleration to large-scale vector supercomputing.

Stäubli Tec-Systems GmbH Connectors: Refresh your Ideas about Thermal Management
Jean-Christophe Duisit (Stäubli Tec-Systems GmbH Connectors)

Thermal management has always been an important topic in electronic. Since cooling with air is reaching the limits now, liquid is becoming the technology adopted. Using liquid, one of the concerns is the serviceability of the systems: both liquid and electronic components are not compatible! By this fact, Quick disconnect are becoming key components and this is where Stäubli brings his expertise. Reliability, high quality machining, series test, flush face design, cleanliness of fluid…. All those different aspects are some strong points to consider when adopting liquid cooling. Working with different industries using liquid cooling, Stäubli has developed a strong experience to designed quick disconnect that can be disconnected without loss of fluid. By working closely as a partner with our customers, Stäubli brings his

expertise to integrates quick disconnect in different configurations: at rack level with blind mate connection, at manifold level or on the Cooling Distribution Unit. The Stäubli group brings to this industry a worldwide network to be able to manage global projects, servicing thermal management teams as well as industrial teams, to bring know how, suggestion, service, in order to have liquid cooling adopted with confidence and safety.

Google Cloud: Democratizing HPC
Ilias Katsardis (Google Cloud)

Google's stated mission is "to organize the world's information and make it universally accessible and useful", and in that spirit, at Google Cloud we strive to have the epitome of latest technological achievements, whether that be GPUs, CPUs, TPUs or even software breakthroughs, and make them meaningfully and sustainably accessible to everyone, anywhere in the world.

IBM: Redefining Computational Science
Oliver Oberst (IBM)

This talk is an overview on how Computational Science will totally change thanks to accelerated system by blurring the lines between HPC and AI. It will also provide an outlook on how Quantum Computers could be leveraged to accelerate certain HPC workloads e.g. in Quantum Chemistry.

Cray: How Exascale Will Change the Enterprise
Brandon Draeger (Cray)

The dawn of the exascale era has arrived and will be marked by new applications that leverage both HPC and AI at extreme scale. These data-centric applications bring the promise of new scientific innovations across multiple research disciplines that will have a tremendous impact for decades to come. Beyond these discoveries, exascale will also drive new breakthroughs in tools and approaches for HPC, AI, and other analytics methodologies as they converge in their usage. The benefit of these learnings will inform not just the future of research computing, but the commercial enterprise as well. In this talk, Cray will share its point of view on the impact, challenges, and benefits of exascale on the enterprise datacenter and share examples of how companies can prepare for this next era of computing.

Dell EMC: Making Innovation Real with High Performance Computing and AI
Thierry Pellegrino (Dell EMC)

With the convergence of HPC and AI, Dell's strategy remains steady, advancing HPC with a world-class

community of experts, democratizing HPC with vertical solutions, and optimizing HPC with HPC investments and the industry's broadest portfolio from workstations to the cloud with Dell Technologies.

Rescale: Incremental or Transformational HPC Cloud Strategies - A Comparison of Scheduler-Based and Platform-Based approaches
Gabriel Broner (Rescale)

Cloud is becoming a reality in HPC and there are two distinct routes organizations are taking to adopt this revolutionary technology:

- In one approach, job schedulers are modified such that jobs can be diverted to cloud infrastructure when given criteria are met.

- In another popular approach, a native HPC cloud platform offers a fully managed multi-cloud environment in a single pane of glass.

Where scheduler-based approaches are incremental in form and impact, platform approaches are transformational as they are fundamentally designed for HPC in the cloud as a compute destination.

This talk will reflect on platform vs. scheduler approaches to HPC in the cloud and will compare the benefits and drawbacks of each approach. Key decision topics such as migration, multi-cloud support, performance, access to applications, licensing, hardware diversity, administration and architecture recommendation are discussed in detail

RSC Group: Next Generation of Hyper-Converged and Ultra-Compact RSC Tornado Solution for the Most Demanding Workloads
Alexey Shmelev (RSC Technologies, RSC Group)

RSC Group, a leading Russian and worldwide well-known developer and integrator of ultrahigh-dense, scalable and energy efficient solutions, introduces at ISC'19 a next generation of hyper-converged and ultra-compact 100% 'hot water' liquid cooled RSC Tornado solution for the most demanding workloads including traditional HPC, Data Center and Cloud, ML/DL/AI applications, Big Data and Distributed Data processing.

It is based on the newest 2nd Generation Intel Xeon Scalable processors (code-named Cascade Lake earlier), Intel Optane DC persistent memory, Intel SSD 'ruler' form factor (EDSFF, Enterprise & Datacenter SSD Form Factor), Intel Optane SSDs and Intel SSDs (NVMe) as well as Intel Server Boards and Intel Omni-Path Architecture high-speed fabric.

Integrated RSC BasIS end-to-end datacenter management platform provides an efficient cluster monitoring and maintenance automation, and was recently enhanced to offer a storage-on-demand solution to the users.

Next presentation starts at 01:40 pm

One Stop Systems: How OSS is Leading the Movement for AI on the Fly™
Jim Ison (One Stop Systems)

AI on the Fly™ is the next killer application for High Performance Computing technology. OSS is a custom manufacturer of specialized high performance computing systems for industries that are showing the largest proliferation of use cases for "AI on the Fly." These industries include deep learning, transportation, security, manufacturing, retail, and media & entertainment.

These edge applications have unique requirements over traditional embedded computing. There is no compromise possible in delivering high performance while maintaining efficient space, weight and power. Delivering the high performance required in edge applications necessitates PCIe interconnectivity providing the fast data highway between high speed processors, NVMe storage and compute accelerators using GPUs or application specific FPGAs. ‘AI on the Fly’ high performance applications will naturally demand this capability on the edge. Additionally, these solutions often require unique space and power saving form factors and specialized rugged enclosures.Why is deep learning training only done in the datacenter and inferencing only done in the field when high performance computers that can be deployed in the field exist today?

To identify hostile threats from planes or on the battlefield, predicting maintenance requirements at the oil field or piloting autonomous vehicles that learn on-the-fly instead of in a datacenter, these applications require local high performance processing. The need to acquire vast quantities of data at ever faster rates and then apply sophisticated analysis algorithms in real time requires all the traditional capabilities of High Performance Computing but now deployed at the edge and in mobile platforms.

Xilinx: Adaptable Acceleration Platforms for Datacenter Applications
Viraj R Paropkari (Xilinx Inc)

The emergence of cloud computing has radically transformed almost every major industry. Exponential growth of compute requirements within cloud computing environments is now driving the need for

heterogeneous computing architectures, which rely on accelerators to deliver power efficient scaling of compute performance. Further compounding the computing challenges is the dawn of AI and the explosion in the sheer amount of data that needs to be stored and processed. A new class of compute and storage acceleration platforms are needed to enable tomorrow's exabyte-scale datacenters. The compute and storage node requires intelligent network fabric to communicate to each other. These accelerators will need to be easy to deploy and manage, and highly adaptable to the ever changing workloads within cloud environments. This talk will focus on Xilinx FPGA based accelerator platforms in Compute, storage , networking and relevant application case studies in HPC , Datacenter applications.

Advania Data Centers - The new way of consuming flexible HPC
Gisli Kr (Advania Data Centers)

Executing HPC in a cloud can be a tricky beast to tame and even though many organizations push for HPC execution in the cloud it comes with challanges. How can you start using fully managed HPC as a Service without disrupting your organizations processes and the way your users work without increasing cost and sacrificing expert support and knowhow?

Western Digital: Understanding Access Patterns in Machine Learning
Manfred Berger (Western Digital)

Abstract will be published shortly

Microsoft: Enabling Rivers of Data Deeply Integrating Cray into Azure
Rob Walsh (Microsoft)

We do this by tightly integrating Cray technology into Azure that is tuned and isolated for specific customer needs. While at the same time allowing them to connect to all native Azure services. This allows clients to leverage all of the agility of Azure and enhance the data being generated by Cray super computers by leveraging those services. This means we can put the largest super computers next to the rest of Azure for large scale data movement.

Boston Limited: Cloud and Clusters: The API Driven HPC Future
David Power (BOSTON)

For decades, storage and networking architectures have been designed according to the limitations of the other as either one or the other would always be the cause of a bottleneck. For instance, switching from HDD to SSD improved storage performance but the network wasn't able to keep up. Developments

in network speed (Ethernet - Fibre Channel - Infiniband) on the other hand, required faster SSDs and new protocols such as NVMe-based SSDs. The industry has now reached a point where this too and fro is no longer necessary as new, software-defined architectures are designed in such a way that storage and networking can fully leverage each other's innovation.

Fujitsu
Pierre Lagier (Fujitsu)

to be submitted

Inspur
Vangel Bojaxhi (Inspur)

Vangel Bojaxhi will give a brief introduction of ASC and let us have a glance at the history of ASC. And then he will also call for ASC2020.

Marvell Semiconductor, Inc.: Bringing Innovation to the HPC Space with ThunderX2 Processors
Craig Prunty (Marvell Semiconductor, Inc.)

Marvell has established a clear leadership position in bringing Arm® -based compute solutions to the High Performance Computing and data center market. This year at ISC, Marvell will provide exciting updates on our product strategy and in particular, we will provide more details on our Marvell ThunderX2® processor family.

EXTOLL GmbH: Next Generation Network Attached Memory within the DEEP-EST Project
Dirk Frey (EXTOLL GmbH)

The Network Attached Memory (NAM) concept was first introduced in the European project DEEP-ER and provided network accessible volatile storage. The first generation had 2GB of Hybrid Memory Cube (HMC) storage, was used to accelerate the DEEP-ER Checkpoint-Restart protocol and provided shared memory for compute resources.

The NAM will be significantly enhanced in DEEP-EST to support higher memory-capacity, and enable more flexible programmability of NAM processing resources. To provide high capacity (up to multiple TB per NAM) and bandwidth (enabling wire-speed access), different memory technologies will be used, in particular LR-DDR4 DRAM, and NAND Flash as NVMe attached devices.

The NAM exploits the EXTOLL high-performance interconnect technology to access compute nodes. A custom Xilinx Kintex UltraScale+ FPGA design provides the NAM core functionality as well as the interfaces to the DDR4 and NVMe modules.

The talk will introduce the NAM design, describes its internal architecture and its application in the DEEP-EST environment.

Focus Session

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Monday, June 17th

Room: Panorama 2, 3
9:00 am - 9:30 am

Opening Session

Welcome & Introduction ISC 2019
Martin Meuer (ISC Group), Thomas Meuer (ISC Group)

ISC 2019 Program
Yutong Lu (NUDT, National Supercomputer Center in Guangzhou)

Announcement of the Two Finalists of the Hans Meuer Award & Announcement of the GCS Award
Saday Sadayappan (The Ohio State University, Department of Computer Science and Engineering)

PRACE – In Service for HPC in Europe
Thomas Lippert (Jülich Supercomputing Centre, FZ Jülich)

Room: Panorama 2, 3
11:00 am - 11:45 am

TOP 500

TOP500, Green500 & HPCG Awards
Horst Simon, Jack Dongarra, Wu Feng, Martin Meuer, Erich Strohmaier, Michael A. Heroux

Highlights of the 53rd TOP500 List
Erich Strohmaier

Room: Panorama 2
4:00 pm - 5:00 pm

Post-K Activities

Post-K Introduction
Mitsuhisa Sato

to be announced soon

Post-K Supercomputer Development
Toshiyuki Shimizu (Fujitsu Limited)

Fujitsu has provided supercomputers for over forty years; high-end supercomputers and x86 clusters supporting wide application areas and customer requirements. RIKEN and Fujitsu are now developing the “post-K” supercomputer as Japan’s new national supercomputer project. The post-K targets up to 100 times higher application performance with superior power efficiency. The post-K employs the newly developed FUJITSU A64FX CPU featuring the Armv8-A and SVE ISA and widening application opportunities. The post-K contributes to the Arm ecosystem for HPC applications as well as science and society. At ISC19, Fujitsu will provide updates on post-K development and some performance evaluation results.

Post-K Software Stack

Yutaka Ishikawa (RIKEN)

In this short presentation, we will present an overview of the Post-K system software stack being developed by the project. It includes a rich set of programming environment, including Fortran, C/C++, OpenMP, Jave, etc., a novel operating system for general-purpose manycore architectures, low-level communication and MPI libraries, and file I/O middleware.

Post-K Co-Design and Applications
Kengo Nakajima (RIKEN R-CCS, The University of Tokyo), Hirofumi Tomita (RIKEN R-CCS)

During development the Post-K computer, highest priority will be given to creating a system capable of contributing to the solution of various scientific and societal issues. For this, the hardware and software will be developed in a coordinated way (Co-design), with the aim to make it usable in a variety of fields. Nine social and scientific priority issues to be tackled by using the Post-K computer are, (a) Achievement of a society that provides health and longevity (1. Innovative drug discovery infrastructure through functional control of biomolecular systems, 2. Integrated computational life science to support personalized and preventive medicine), (b) Disaster prevention and global climate problems (3. Development of integrated simulation systems for hazards and disasters induced by earthquakes and tsunamis, 4. Advancement of meteorological and global environmental predictions utilizing observational “Big Data”), (c) Energy problems (5. Development of new fundamental technologies for high-efficiency energy creation, conversion/storage and use, 6. Accelerated development of innovative clean energy systems), (d) Enhancement of industrial competitiveness (7. Creation of new functional devices and high-performance materials to support next-generation industries（CDMSI）, 8. Development of innovative design and production processes that lead the way for the manufacturing industry in the near future) and (e) Development of basic science (9. Elucidation of the fundamental laws and evolution of the universe). In this talk, achievements of these 9 priority issues and efforts towards Co-design will be described.

Room: Panorama 3
4:00 pm - 5:00 pm

Containers for Acceleration and Accessibility in HPC and Cloud Ecosystems

Session Description: Applications portability, scientific reproducibility and users productivity are among key challenges facing scientific communities on rapidly evolving hardware and software ecosystems, especially for workflows utilising distributed IT infrastructure encompassing public and private cloud deployments and supercomputing centres. Container technologies have demonstrated not only a widespread adoption among data science communities in cloud environments but also unique problem-solving opportunities for performance-sensitive, scalable applications in modelling and simulation

domains on supercomputing platforms. This session brings together experts to share insights on transitioning to container technologies, and to forecast opportunities and challenges for a federated IT environment comprising HPC and cloud infrastructure elements.

High-Performance Data-Intensive Science: Clouds, Containers, Workflows, and the Data Lifecycle
Arjun Shankar (Oak Ridge National Laboratory, National Center for Computational Science)

The HPC environments of tomorrow will have to flexibly accommodate new application domains and dynamic connections with peer facilities. We already see the need to accommodate data-driven applications at scale for AI and campaigns with interleaved simulation and analytics. Data availability from simulations or observational data sources is particularly relevant to enable AI applications at scale. Computing facilities have taken the logical step of instantiating Cloud and Container orchestration frameworks adjacent to the core HPC systems. Such constructs enable key classes of workflows that provide persistence of control while supporting traditional HPC paradigms of computing. We report on our early experiences using such an approach and discuss how this can apply to create seamless connections within and across facilities. The underlying data lifecycle provides the backdrop for such data-intensive scientific explorations.

Introducing Container Technology to TSUBAME3.0 Supercomputer
Akihiro Nomura (Tokyo Institute of Technology)

We report usage of container technology in TSUBAME3.0, production supercomputer located at Tokyo Institute of Technology, from both operator and user views. When we introduce software into a running production system, we have to be extremely careful with privileged operations to prevent the invasion to other users secret data. Also, when we run parallel applications in the container environment with native protocols of InfiniBand or OmniPath, we need to prepare appropriate system software to both outside and inside of the container. Considering those performance and security concerns, we finally decided to introduce Docker and Singularity to TSUBAME3.0 with certain restrictions. We also give a case study report from Singularity user in TSUBAME3.0.

Tuesday, June 18th

Room: Panorama 2
8:30 am - 10:00 am

Memory, New Technologies and Bandwidth Challenges for Future HPC-Systems

Session Description: Advanced device technologies such as 3D-stacked memory and non-volatile random-access memory (NVRAM) have added a new dimension to the already over complex memory hierarchies in high-performance computing (HPC) systems. This is new dimension provides new possibilities to meet the increasing demand of big data applications and to address the notorious memory-wall problem. Computer hardware systems, operating systems, storage and file systems, data models and programming stacks, performance models and tools need to be enhanced, augmented, or even redesigned to address the performance, programmability and energy efficiency challenges to support an integrated deep memory-storage hierarchy for HPC and data-intensive applications. In this session, the speakers will share their experiences and findings in addressing emerging memory challenges for exascale computing. This session is anticipated to help the HPC community understanding the scope of modern memory system research and identifying future research directions to address memory and storage challenges via advanced technologies and emerging systems.

Extreme Heterogeneity in Emerging Memory Systems
Jeffrey Vetter (Oak Ridge National Laboratory, University of Tennessee)

Concerns about energy-efficiency and cost are forcing the US Exascale Computing Project to reexamine system architectures, and, specifically, the memory and storage hierarchy. While memory and storage technologies have remained relatively stable for nearly two decades, new architectural features, such as deep memory hierarchies, non-volatile memory (NVM), and near-memory processing, have emerged as possible solutions. However, this era of extreme heterogeneity in memory systems will have a major impact on HPC software systems and applications. To be effective, software and applications will need to be redesigned to exploit these new capabilities. In this talk, I will sample these emerging memory technologies, discuss their architectural and software implications, and describe several new approaches to programming these systems. One such system is Papyrus (Parallel Aggregate Persistent -yru-Storage); it is a programming system that aggregates NVM from across the HPC system for use as application data structures, such as vectors and key-value stores, while providing performance portability across emerging NVM hierarchies.

Performance Portability with Data-Centric Parallel Programming
Torsten Hoefler (CSCS / ETH Zurich)

The ubiquity of accelerators in high-performance computing has driven programming complexity beyond the skill-set of the average domain scientist. To maintain performance portability in the future, it is imperative to decouple architecture-specific programming paradigms from the underlying scientific computations. We present the Stateful DataFlow multiGraph (SDFG), a data-centric intermediate representation that enables separating code definition from its optimization. We show how to tune several applications in this model and IR. Furthermore, we show a global, datacentric view of a state-of-the-art

quantum transport simulator to optimize its execution on supercomputers. The approach yields coarse and fine-grained data-movement characteristics, which are used for performance and communication modeling, communication avoidance, and data-layout transformations. The transformations are tuned for the Piz Daint and Summit supercomputers, where each platform requires different caching and fusion strategies to perform optimally. We show that SDFGs deliver competitive performance, allowing domain scientists to develop applications naturally and port them to approach peak hardware performance without modifying the original scientific code.

Memory Technology Impacts on Current, Near-Term, and Future Systems
Ron Brightwell (Sandia National Laboratories)

For many applications, memory continues to be the latency and bandwidth bottleneck. A wide variety of emerging memory technologies and architectures are attempting to alleviate these constraints, but they face substantial hurdles in providing enough useful bandwidth to the processor. This talk will show recent performance results from the Sandia Astra system, which is currently the largest Arm-based HPC system. Many of these results can be attributed to the increased memory bandwidth available on the system. We will also present results from a recent study by the US DOE Exascale Computing Project Memory Working Group to evaluate future improvements to High Bandwidth Memory technology. Finally, we will explore several complementary efforts to improve the performance of HPC systems by adding accelerators with a memory focus.

Deep Memory-Storage Hierarchy and Pace-Matching Data Access
Xian-He Sun (Illinois Institute of Technology)

Computing has changed from compute-centric to data-centric. From deep-learning to visualization, data access becomes the main performance concern of computing. In this talk, based on a series of fundamental results and their supporting mechanisms, we introduce a new thought on memory system design. We first present the Concurrent-AMAT (C-AMAT) data access model to quantify the unified impact of data locality, concurrency and overlapping. Then, we introduce the pace-matching data-transfer design methodology to optimize memory system performance. Based on the pace-matching design, a memory-storage hierarchy is built to generate final results and to mask the performance gap between computing and data transfer. C-AMAT is used to optimize performance at each memory layer, and a global management algorithm, named Layered Performance Matching (LPM), is developed to optimize the overall performance of the memory system. The holistic pace-matching optimization is very different from the conventional locality-based system optimization and is especially powerful in a dynamic heterogeneous environment. A deep memory-storage hierarchy system is designed to carry the pace-matching optimization. Experimental testing confirms the theoretical findings, with a 150x reduction of memory stall time. We will present the concept of the pace-matching data-transfer design and some case studies on DoE and NASA applications. We will also discuss our current NSF funded DMSH projects as

well as general research issues related to advanced memory systems.

Room: Panorama 3
8:30 am - 10:00 am

Mixed Precision (Hardware and Software Interface)

Posits and Quires: Freeing Programmers from Mixed-Precision Decisions

*John L. Gustafson (A*STAR, National University of Singapore)*

With the slowing of Moores law speed improvements, HPC programmers are discovering that trimming the unnecessary use of 64-bit floating-point representation can increase speed, lower energy/power costs, and relieve bandwidth bottlenecks. However, 32-bit IEEE floats often have too little accuracy for HPC tasks, and choosing where to use them is a burden for programmers.

Posit representation has more information-per-bit than IEEE floats, and 32-bit posits have proved 10 to 30 times as a accurate as 32-bit floats; moreover, they are backed by a Kulisch-style exact dot product, finally made practical by requiring only 512 bits (the "quire" register) instead of the thousands of bits needed in the past. Intel's AVX-512 vector instructions show that modern microprocessors are already up to the task of handling 512-bit quantities. Support for the quire means a compiler can automatically invoke iterative methods where higher precision is needed instead of requiring the programmer to make (risky) choices and decisions and complicate the code. Similarly, 16-bit posits have been shown to be very effective replacements for 32-bit floats, even for chaotic systems like weather and climate models. The quire provides a mathematically perfect way to measure the residual in solving systems of equations, so even 16-bit posits can sometimes outperform 64-bit floats at linear algebra operations.

With the emerging Posit Standard, which includes the quire, the benefits of mixed precision arithmetic need not create an additional burden for programmers. It can be, and should be, automatic.

Variable Precision Computing Strategies

Jeffrey Hittinger (Lawrence Livermore National Laboratory)

Today, we typically compute and store results in 64-bit double precision by default, even when very few significant digits are required. Because of the growing disparity of FLOPs to memory bandwidth in modern computer systems and the rise of General-Purpose GPU computing – which has better peak performance in half and single precision on some hardware – there has been renewed interest in computing in precisions other than double. The reality is that many of the bits in double precision are

representing errors – truncation, iteration, and roundoff – instead of useful information about the solution. This over-allocation of resources is wasteful of power, bandwidth, storage, and FLOPs; we communicate and compute on many meaningless bits and do not take full advantage of the computer hardware we purchase.

At LLNL, we are developing the methods and tools that will enable the routine use of dynamically adjustable precision at a per-bit level depending on the needs of the task at hand. Just as adaptive mesh resolution frameworks adapt spatial grid resolution to the needs of the underlying solution, our goal is to provide more or less precision as is needed locally. Acceptance from the community will require that we address three concerns: that we can ensure accuracy, ensure efficiency, and ensure ease of use in development, debugging, and application. In this talk, I will discuss the benefits and the challenges of variable precision computing, highlighting aspects of our ongoing research in data representations, numerical algorithms, and testing and development tools.

Exploring Alternative Numerical Formats Using Reconfigurable Architectures
Artur Podobas (RIKEN Center for Computational Science)

The inevitable end of Moore's law motivates researchers to re-think many of the historical architectural decisions. Among these decisions we find the representation of floating-point numbers, which has remained unchanged for nearly three decades. Chasing better performance, lower power consumption or improved accuracy, researches today are actively searching for smaller and/or better representations. Today, a multitude of different representations are found in the specialized (e.g. Deep-Learning) applications as well as for general-purpose applications (e.g. POSITs).

However, despite their claimed strengths, alternative representations remain difficult to evaluate empirically. There are software approaches and emulation libraries available, but their slowness only allows the smallest of data-sets to be evaluated and understood.

In this talk, I will show how we have described the POSIT representation using hardware description languages and embedded it into the well-known OpenCL programming model, ready to be accelerated using reconfigurable architectures. Our approach allows us to reach the performance levels required to start evaluating large workloads empirically, which will be illustrated with use-cases we have explored.

Room: Panorama 2
11:00 am - 12:30 pm

State-of-the-Art in Quantum Computing Works

The Dawn of Superconducting Quantum Processors

Irfan Siddiqi (UC Berkeley, Lawrence Berkeley National Laboratory)

Quantum coherence can now be observed for longer than 100 microseconds in superconducting chips containing tens of physical qubits comprised of Josephson tunnel junctions embedded in resonant microwave circuitry. Combining such long-lived coherence with quantum-noise-limited, broadband detection of weak microwave signals has enabled the realization of nascent quantum processors suitable for executing shallow-circuit quantum algorithms with modest gate counts and minimal error mitigation. As an example, I will describe the implementation of a hybrid quantum-classical variational eigensolver with superconducting transmon qubits to determine the ground and excited states of simple molecules with near-chemical accuracy, and a teleportation protocol using ternary logic to simulate scrambling processes in black holes.

Opportunities and Challenges of Quantum Computing

Damian Steiger (Microsoft)

We are currently in the early development stage of quantum computers, which are based on using the concepts of quantum mechanics to do computation. They promise to solve problems that are intractable on classical computers, such as factoring numbers or the exact simulation of molecules and materials. However, while quantum computers are universal computers, they are best viewed as special purpose accelerators for only specific problem classes because of their inherent limitations. In this talk, I will attempt to present a realistic assessment of the current quantum computing hardware and the potential of these devices for, e.g., the simulation of quantum systems. Moreover, I will shortly show how quantum computing has already influenced the development so called quantum inspired optimization (QIO) algorithms which run on classical hardware.

Combinatorial Optimization with Quantum Computers

Mario Szegedy (Alibaba Inc.)

Combinatorial Optimization Problems arise in several branches of industry and science, where they are known to be notoriously demanding on computational resources. There are also several attempts to tackle them with quantum computers. We compare existing methods. Some analyses are done with the tools that our quantum team has developed.

Room: Panorama 3

11:00 am - 12:30 pm

Programming Models (Exascale)

Performance Portability in the Exascale Era

Simon McIntosh-Smith (University of Bristol)

Multiple different computer architectures are expected to be required to reach the Exascale era. From GPUs to many-core CPUs using heavy weight or light weight cores, this diversity of architectures will create a huge challenge for scientific software developers: how can we write applications which will run efficiently across all these systems? In this talk we will investigate performance portability in the Exascale era, presenting some results from a wide-scale study of performance portability. We will also examine the performance portability implications of architecture classes such as GPUs and many-core CPUs, as well as the effect that the choice of parallel programming language may have.

The OpenMP API at the Dawn of Exascale

Michael Klemm (OpenMP Architecture Review Board, Intel Deutschland GmbH)

Since its creation in 1997, the OpenMP API has become the standard programming model for on-node parallelism in HPC applications and has enabled many scientific discoveries by making it easy for scientists to exploit the power of modern computers. The OpenMP API uses directives to augment code written in C/C++ and Fortran with parallelization, vectorization, and offload instructions for the compiler.

Version 5.0 of the OpenMP API introduced major enhancements and includes many powerful parallelization features for modern multi-threaded applications. In this presentation, we will review the major additions for multi-threading and support of heterogeneous programming. We will then provide an overview of the features planned for future OpenMP versions and how the OpenMP API can provide a directive-based yet powerful parallelization paradigm in the Exascale era.

Parallel Programming - Painful or Productive?

Sandra Wienke (RWTH Aachen University)

In pursuit of exascale computing, the complexity of parallel hardware architectures will increase and, hence, will the complexity of software development of scientific applications. Developers will spend painfully more effort to parallelize applications or port them to new hardware architectures. Thus, besides expenses for hardware and power consumption, we need to consider 'brainware' costs when moving to the exascale era.

In this talk, we look at parallel programming models in terms of software development effort and productivity. Based on human-subject studies, the effort-performance tradeoff in parallel programming

can be evaluated. Scaling such results to an HPC center's perspective, we can get insights to the center's cost effectiveness.

Room: Panorama 2
1:45 pm - 3:15 pm

Challenges & Visions for Future Exascale Systems

Update on Post-K Development

Yutaka Ishikawa (RIKEN)

The next flagship supercomputer in Japan, replacement of the K supercomputer and thus we call it post-K computer, is being developed since 2014. The general operation will start in early 2021. Its node architecture and interconnect are Armv8-A SVE and a 6-D mesh/torus network, respectively. The design of CPU, system configuration, and its software stack has been completed. After updating some aspects of CPU and system configuration, the system software developed in the post K supercomputer, including a novel operating system for general-purpose manycore architectures, low-level communication and MPI libraries, and file I/O middleware, will be introduced.

Flexibly Scalable Exascale Architectures with Embedded Photonics

Keren Bergman (Columbia University)

Computing systems are critically challenged to meet the performance demands of applications particularly driven by the explosive growth in data analytics. Data movement, dominated by energy costs and limited ‘chip-escape’ bandwidth densities, is a key physical layer roadblock to these systems’ scalability. Integrated silicon photonics with deeply embedded optical connectivity is on the cusp of enabling revolutionary data movement and extreme performance capabilities. Beyond alleviating the bandwidth/energy bottlenecks, embedded photonics can enable new disaggregated architectures that leverage the distance independence of optical transmission. We will discuss how the envisioned modular system interconnected by a unified photonic fabric can be flexibly composed to create custom architectures tailored for specific applications.

Practical Solutions to Programming for Performance

William D. Gropp (University of Illinois at Urbana-Champaign)

High-end computing has benefited from decades of architectural stability. That stability ended with the

end of Dennard scaling, leading to rapid and continued innovation in computer architecture. This innovation is creating challenges for exascale systems that are different than the challenges for the extreme scale systems of the past. A characteristic of extreme scale systems has been their scale, with systems having many thousands of nodes, each with tens to hundreds of cores. Handling scale is a challenge for both applications and algorithms, but often a bigger challenge is achieving high performance on increasingly complex nodes. And while the commodity market is also challenged by this node complexity, the software tools for that market do not emphasize high-end performance. This talk discusses the challenges and possible solutions for intranode as well as internode programming, with an emphasis on building upon successful programming systems and language in both high end and commodity computing.

Exascale Systems Present a Vision for Weather and Climate Prediction - Can we Meet the Challenges?
Peter Bauer (ECMWF)

A qualitative change of our models towards much enhanced predictive skill requires running simulations at much finer resolutions than today, with more realistic Earth-system models and with much larger ensembles. Our data assimilation methods need to follow this trend to provide accurate initial conditions at such scales exploiting information from unprecedented volumes of observational data. Meeting these requirements translates into at least 1000 times bigger high-performance computing and data management resources than available today – towards what's generally called 'exascale'. However, our current codes only reach about 5% efficiency on supercomputers so that we are actually far away from true exascale computing. Achieving the next step in forecasting therefore needs a significant investment in code efficiency, which entails one of the most radical changes in weather and climate prediction since the first implementation of numerical techniques on computers in the 1950s. This step encompasses a fundamental redesign of mathematical algorithms and numerical methods, the adaptation to new programming models, the implementation of dynamic and resilient workflow management, and the efficient post-processing and handling of big data. While artificial intelligence methods cannot overcome the main bottlenecks of efficient computing they can help alleviate algorithmic cost and support information extraction from both observational and simulated data. The weather and climate community is increasingly becoming connected to rethink their approach to efficient forecasting - as this challenge is too big to be solved by individual organisations or communities.

Room: Panorama 3
1:45 pm - 3:15 pm

Extreme-Scale Earth System Modeling

Designing Finite Element Multigrid Solvers for Extreme-Scale Earth Mantle Convection Simulations

Nils Kohl (Friedrich-Alexander-University Erlangen-Nuremberg (FAU)), Ulrich Rüde (Friedrich-Alexander-University Erlangen-Nuremberg (FAU), CERFACS Toulouse)

Insightful, finely resolved simulations of physical models such as Earth-mantle convection require the solution of systems of equations of enormous size. A global resolution of the Earth-mantle of about 1km results in more than a trillion (10^{12}) unknowns. Only solvers with optimal complexity - such as multigrid methods - can achieve that scalability.

In this talk we present the HPC framework HyTeG that implements parallel and matrix-free finite-element multigrid solvers for extreme-scale simulations as they are required for modern geophysical applications. We combine excellent performance, scalability and geometric flexibility through structured refinement of unstructured meshes and fully distributed domain partitioning.

Seismic Simulations Using the ExaHyPE-Engine

Anne Reinarz (Technical University of Munich)

ExaHyPE is a hyperbolic PDE engine for solving systems of first order hyperbolic PDEs written in a conservative or non-conservative form. In this talk, I present the current status of the ExaHyPE project in general and in particular the parallel capabilities of the engine. The project provides a space-tree discretization of the computational domain, various higher-order DG schemes and a-posteriori subcell limiters. This allows users to write only their own application specific code and benefit from the engines efficient adaptive mesh refinement algorithms and from the numerical schemes built into the engine.

The two main applications currently tackled with this engine are long-range seismic risk assessment and the search for gravitational waves emitted by binary neutron stars. In this talk I will focus on the seismic simulations and show two methods that allow us to resolve complex geometry in spite of our reliance on cartesian meshes.

This is joint work with groups from Frankfurt's FIAS, the University of Trento, Ludwig- Maximilians-University Munich and the University of Durham.

Efficient Discontinuous Galerkin Solvers for Groundwater Problems on Modern CPU Architectures

Steffen Müthing (Heidelberg University, IWR)

In order to deliver meaningful answers to real-world problems, modern earth system simulations need to

model increasingly large geographical areas at a high resolution, driving a need for high performance and scalability. Discontinuous Galerkin methods are a good fit for simulations in this field, posessing beneficial mathematical properties and being well suited for modern architectures. We present our high-performance DG approach that combines a matrix-free DG solver with an AMG-based low-level subspace correction, which achieves very high efficiency on modern CPU architectures.

Hand-coding the required high-performance kernels does not scale well to application scientists such as geophysicists, who want to focus on their research topics instead of implementation details. In order to alleviate this problem, we are developing a code-generation framework that allows application scientists to formulate their problem in a high-level DSL. We will demonstrate some of the unique optimization opportunities afforded by this approach, as we are able to apply additional problem knowledge at different stages of the code generation process, which allows us to perform optimizations that would not be possible in a general-purpose code.

Room: Panorama 2
3:45 pm - 4:45 pm

High Performance Computing in 2029 or The Cambrian Explosion in Computing in the 2020s

High Performance Computing in 2029 or The Cambrian Explosion in Computing in the 2020s
John Shalf (Lawrence Berkeley National Laboratory), Kristel Michielsen (Jülich Supercomputing Centre (JSC), RWTH Aachen University), Yutong Lu (National Supercomputer Center in Guangzhou), Kengo Nakajima (University of Tokyo, Supercomputing Research Division, Information Technology Center; RIKEN R-CCS), Jack Dongarra (University of Tennessee, Oak Ridge National Laboratory)

The next decade promises to be one of the most exciting yet in the further evolution of computing. There are a number of developments that will change how we will compute in 10 years: the foreseeable end of Moore's law will lead to the exploration of new architectures and the introduction of new technologies in HPC; the rapid progress in machine learning in the last decade has led to a refocus of HPC towards large scale data analysis and machine learning; the feasibility of quantum computing has led to the introduction of new paradigms for scientific computing; meanwhile 30 billion IOT devices will push advances in energy efficient computing and bring an avalanche of data. I would like to compare the situation to a Cambrian explosion: the change in computing environment has helped creating a wide and complex variety of "organisms" that will compete for survival in the next decade. The HPC community will have to deal with this complexity and extreme heterogeneity, and decide what ideas and technologies will be the survivors. In this panel, I will ask several worldwide HPC experts to make their predictions for 2030.

Room: Panorama 3
3:45 pm - 4:45 pm

Computational Neuroscience and Neuromorphic Computing: Foundations of Next-Generation Artificial Intelligence

Session Description: The recent progress in artificial intelligence is inspired by early insights into brain function. However, the fundamental interaction between neurons and the architecture of the mammalian brain differ radically from present AI hard- and software. Neurons communicate by point-like events, called spikes, where mainly the timing carries information and each neuron emits only a few spikes per second. The brain is hierarchically organized but at the same time highly recurrent on multiple scales. While a neuron receives input from about ten thousand others, the vast network size leads to a very low connection probability. Thus, computation is extremely sparse in space and time; the opposite of computationally dense matrix operations. The field studying the dynamics and function of neuronal networks is computational neuroscience. The field of neuromorphic computing investigates how a computer can be built based on the fundamental interactions and architecture of the brain. Systematic integrated funding has brought Europe into a world-leading position. The contributors to this session work together in the Human Brain Project (HBP). After a brief introduction to the topic by Markus Diesmann, Susanne Kunkel will discuss the state of the art in the simulation of brain-scale neuronal networks on conventional supercomputers on the example of the NEST code. Subsequently, Steve Furber will demonstrate the design and capabilities of the SpiNNaker neuromorphic hardware, highlighting the one-million-core installation in Manchester. Finally, Mihai Petrovici will present progress on spike-based computation. Together, the talks show how computational neuroscience and neuromorphic computing create the foundations for the next-generation AI.

Routing Brain Traffic through the Bottlenecks of General Purpose Computers: Challenges for Spiking Neural Network Simulation Code

Susanne Kunkel (Norwegian University of Life Sciences (NMBU))

Simulation of spiking neuronal networks on general purpose computers is a third pillar supporting the investigation of the dynamics and function of biological neural networks, next to experimental and theoretical approaches. In recent years, ever more scalable simulation code has been developed that works efficiently for a broad variety of models and on various platforms, from laptops to supercomputers. The challenges for neuronal simulators on general purpose computers arise from the sparse but broad connectivity in neuronal network models and from the unpredictable pulse signaling of neurons, called spiking. In distributed simulations of such networks, this requires frequent communication of spike data from varying sources to varying targets, which is a principle complication for the efficient exchange of

data between processes. Moreover, routing of the spike data received by a process to the local targets entails irregular memory access, which constitutes a major performance bottleneck. My talk will address such challenges for spiking network simulators and present recent developments in simulation technology that aim at meeting these challenges.

Many-Core Neuromorphic Computing with SpiNNaker

Steve Furber (The University of Manchester)

Neuromorphic computing - that is, computing based upon brain-like principles - can be traced back to the pioneering work of Carver Mead in the 1980s. Academic research into neuromorphic systems has continued since then in various forms, including analog, digital and hybrid systems, primarily with the objective of improving understanding of information processing in the brain. More recently, industrial neuromorphic systems have emerged - first the IBM TrueNorth, and then the Intel Loihi - with a greater focus on practical applications. In parallel the last decade has seen an explosion of interest in less brain-like, though still brain-inspired, artificial neural networks in machine learning applications that have, for example, placed high-quality speech recognition systems into everyday consumer use. However, these artificial neural networks consume significant computer and electrical power, particularly during training, and there is strong interest in bringing these requirements down and in enabling continuous on-line learning to take place in self-contained, mobile configurations. There is a growing expectation, so far unsubstantiated by compelling evidence, that neuromorphic technologies will have a role to play in delivering these efficiency gains. The SpiNNaker (Spiking Neural Network Architecture) platform is an example of a highly flexible digital neuromorphic platform, based upon a massively-parallel configuration of small processors with a bespoke interconnect fabric designed to support the very high connectivity of biological neural nets in real-time models. Although designed primarily to support brain science, it can also be used to explore more applications-oriented research.

Computing with physics: from biological to artificial intelligence and back again

Mihai A. Petrovici (Universität Bern, Universität Heidelberg)

Neural networks are, once again, in the focus of both the artificial and the biological intelligence communities. Originally inspired by the dynamics and architecture of cortical networks, they have increasingly strayed away from their biological archetypes, prompting questions about their relevance for understanding the brain. However, their recent hardware-fueled dominance has motivated renewed efforts to align them with biologically more plausible models. In my talk, I will discuss some intriguing ideas about the physical instantiation of information processing in biologically inspired hierarchical neural networks and possible benefits that can be derived therefrom.

Wednesday, June 19th

Room: Panorama 1
8:30 am - 10:00 am

Automatic Code Generation

Beyond ExaStencils
Sebastian Kuckuk (Friedrich-Alexander-University Erlangen-Nuremberg (FAU)), Harald Köstler (Friedrich-Alexander-University Erlangen-Nuremberg (FAU))

Domain-specific languages (DSLs) and code generation techniques have been an active field of research gaining momentum in the last years. The ExaStencils code generation framework and its multi-layered external DSL ExaSlang provide pioneering work in the field of PDE solvers. Their main focus lies on multigrid methods for (block-) structured grids. In this talk, we demonstrate how this approach can be extended to new application domains and how it can be coupled to external tools. For the first part, we implement a solver for the hyperbolic shallow water equations (SWE) discretized with discontinuous Galerkin (DG). Using Python as alternative means of input allows us to express core concepts in a natural way. After performing symbolic manipulations, generation of massively parallel implementations running on CPU and GPU is possible via mapping to ExaSlang. For the second part, we showcase how ExaStencils can be used as an evaluation platform to perform automatic solver composition based on genetic programming.

Firedrake: High Productivity, High Performance Simulation through Code Generation
David Ham (Imperial College, London)

A critical challenge in the numerical solution of PDEs is that the mathematical route from equations to simulation comprises many steps, each of which demands a high degree of sophistication. Choice of equations and discretisation, implementation of local operators, global assembly and parallelisation, low-level code optimisation, solvers, preconditioners: each of these is a domain of expertise in its own right on which theses and books have been written. However the simulation developer necessarily has limited resources and can only be truly expert in some parts of this chain.

Firedrake addresses this challenge by modelling the finite element simulation creation process as a series of mathematical representations, and software which maps between them, automatically transforming the simulation problem from higher to lower mathematical abstractions until high performance compiled code is generated and executed. This makes every stage of the simulation process composable: users can benefit from advanced algorithms at every layer, and can change their choices without reimplementing. By tightly integrating with PETSc's composable solver interface,

sophisticated nested preconditioners which create and solve the appropriate auxiliary differential operators on the fly can easily be created. This composable infrastructure yields a step-change in productivity for users, who become able to create sophisticated optimised PDE solvers much more efficiently than is otherwise possible.

Exploiting Locally Structured Meshes to Achive High Performance for Low Order FEM
Marcel Koch (University of Münster)

Finite element methods (FEM) are among the most commonly used methods for the numerical solution of PDEs. The linear system corresponding to a PDE is usually solved by fully assembling the sparse system matrix. Computations involving sparse matrices are inherently memory bound and thus don't profit from newer CPU improvements. To overcome this, current research investigates matrix free computations, which has been shown to improve computation time for example in higher order DG simulations.

Matrix free computations for low order FEM have a low arithmetic intensity. Therefore this approach is also memory bound. Using locally structured meshes simplifies memory access, which greatly improves the FLOP/s. Furthermore, this allows for additional optimizations, e.g. straight forward cross-element vectorization.

This talk presents a python based approach to generate kernel code for FEM on locally structured meshes. Based on a weak formulation in UFL an intermediate representation in Loo.py of the kernel's loop structure is created. Loo.py allows a wide range of kernel transformation, e.g. tiling, unrolling or explicit vectorization. The resulting C++ kernel is used by DUNE PDELab. This talk presents performance results for different PDEs discretized on structured or unstructured coarse grids.

Abstractions and Domain Specific Language Compilers for Weather and Climate Applications
Carlos Osuna Escamilla (MeteoSwiss)

Weather and Climate simulations are subject of unprecedented scientific interest due to the urgent need to design and adopt efficient climate change mitigation measures. Increasing horizontal resolution to the order of 1km is key to reduce the high uncertainty associated with climate projections. However, the computational cost of running 1km for global models on traditional CPU supercomputers is unaffordable. Therefore, the community must adopt and be able to efficiently exploit performance of modern accelerators and hybrid supercomputing systems. However the diversity and complexity of hardware architectures is imposing a huge challenge for large and complex models that must be ported and maintained for multiple architectures combining various parallel programming models. Several domain-specific languages (DSLs) have been developed to address the portability problem, but they usually support specific numerical methods and impose a fixed parallel programming model that decreases the scientific productivity of the model developer. With a holistic approach to tackle the performance

portability problem of complex Fortran based models, we present new high-level domain specific programming languages that allow to express numerical methods and generate efficient parallel implementations as well code generators that allow to transform existing large and complex models in Fortran. We evaluate and discuss the different approaches based on the GPU operational code of COSMO.

AnyDSL: A Partial Evaluation Framework for Programming High-Performance Libraries
Richard Membarth (DFKI, Saarland University), Roland Leißa (Saarland University)

AnyDSL is a framework for the implementation of domain-specific libraries (DSLs). Library abstractions are designed in Impala, a functional and imperative language. In order to achieve high-performance, Impala partially evaluates any abstractions these libraries might impose. Partial evaluation and other optimizations are performed on AnyDSL's intermediate representation Thorin. This allows to separate the algorithm description from the target hardware mapping, generating highly optimized implementations for CPU, GPU, or FPGA from the same generic, high-level code base. The performance of the generated code is competitive with manual, hand-optimized implementations for many application domains such as image processing, real-time ray tracing, or bioinformatics.

Room: Panorama 2
8:30 am - 10:00 am

New Approaches, Algorithms Towards Exascale Computing

ZFP: Compressed Floating-Point Arrays for Exascale Computing
Peter Lindstrom (Lawrence Livermore National Laboratory)

One of the primary challenges for Exascale computing is overcoming the performance cost of data movement. Through simulation, observation, and experiments, far more data is being generated than can reasonably be stored to disk and later analyzed without any form of data reduction. Moreover, with deepening memory hierarchies and dwindling per-core memory bandwidth due to increasing parallelism, even on-node data motion between RAM and registers makes for a significant performance bottleneck and primary source of power consumption.

zfp is a floating-point array primitive that mitigates this problem using very high-speed, lossy (but optionally error-bounded) compression to significantly reduce data volumes. zfp reduces I/O time and off-line storage by 1-2 orders of magnitude depending on accuracy requirements, as dictated by user-set error tolerances. Unique among data compressors, zfp also supports constant-time read/write random

access to individual array elements from compressed storage. zfp's compressed arrays appear to the user like conventional uncompressed arrays and can often be integrated into existing applications with minimal code changes. When used in numerical computations, zfp arrays provide a fine-grained knob on precision while achieving accuracy comparable to IEEE floating point at half the storage, reducing both memory footprint and bandwidth.

Solving the Sampling Problem in Statistical Mechanics: Using Physical Theory to Obtain Ensemble-Level Parallelism in HPC for Molecular Simulation

Ada Sedova (Oak Ridge National Lab)

Ensemble methods are increasingly being used in molecular simulation to solve the problem of Moore's-law limits on our ability to sample the complete simulation space with physical accuracy. In order to use such methods in statistical mechanics, an appropriate physical theory must be able to provide a means to reduce hundreds to thousands of independent parallel calculations into a physically meaningful result. Methods such as transition-path sampling, replica-exchange, and Markov State Models (MSM), along with simpler solutions such as normal mode analysis, have provided these types of solutions for a number of condensed-matter simulation problems. These methods have recently become highly powerful through the use of HPC. All of these methods require some type of workflow, with a top-layer wrapper that must manage parallel distributed tasks and then reduce the data into some final form. With the increased use of acceleration and parallelization in state-of-the art molecular simulation programs, a workflow must be able to integrate many separate jobs, that each use multiple accelerators (e.g. GPUs), and various levels of parallelism including threading (e.g. OpenMP) and MPI, along with, potentially, multiple nodes each. Managing ensemble-workflows of these types of programs quickly becomes a non-trivial task. This talk discusses different ensemble methods in molecular simulation as well as experiences with software infrastructure solutions within HPC.

Addressing the Communication Bottleneck: Towards a Modular Precision Ecosystem for High Performance Computing

Hartwig Anzt (Karlsruhe Institute of Technology, University of Tennessee)

Over the last years, we have observed a growing mismatch between the arithmetic performance of processors in terms of the number of floating point operations per second (FLOPS) on the one side, and the memory performance in terms of how fast data can be brought into the computational elements (memory bandwidth) on the other side. As a result, more and more applications can utilize only a fraction of the available compute power as they are waiting for the required data. With memory operations being the primary energy consumer, data access is pivotal also in the resource balance and the battery life of mobile devices. In this talk we will introduce a disruptive paradigm change with respect to how scientific data is stored and processed in computing applications. The goal is to 1) radically decouple the data storage format from the processing format; 2) design a "modular precision ecosystem" that allows for

more flexibility in terms of customized data access; 3) develop algorithms and applications that dynamically adapt data access accuracy to the numerical requirements.

Room: Panorama 1
11:00 am - 12:30 pm

Applications for Quantum Computing

Session Description: Nowadays, various types of quantum computing devices with largely varying numbers of qubits are available for pilot users. They have cloud-based access to several gate-based quantum computers (IBM, Google, Riggetti Computing, CAS-Alibaba, …) and to a quantum annealer of D-Wave Systems. Apart from academic interest in quantum computing to simulate quantum many-body systems in physics, materials science and chemistry there is also interest shown by aerospace, automotive, oil and gas, financial, chemical and pharmaceutical industries in this new disruptive computing technology. For these industries, among others, fault tree analysis, risk mitigation, optimization, scheduling, and machine learning play an important role. In this session, apart from an introduction on what can and cannot be done on a quantum computer and quantum annealer, programming experience on and prototype applications of these new computing technologies in science and industry will be discussed.

Quantum Computing and Annealing: What Can and Cannot be Done?
Kristel Michielsen (Jülich Supercomputing Centre, Forschungszentrum Jülich)

Quantum computing promises unprecedented possibilities for important computing tasks such as quantum simulations in chemistry and materials science or optimization and machine learning. The development of novel and efficient methods and algorithms that explicitly take advantage of such emerging disruptive computing architectures is a huge challenge and opportunity.

Quantum algorithms for gate-based quantum computers and quantum annealers are different. On a gate-based quantum computer, a quantum algorithm consists of a sequence of quantum circuit operations (gates) that are performed on the qubits. In case of quantum annealing, a quantum algorithm is the continuous time (natural) evolution of a system of qubits to find the lowest-energy state of a system representing an optimization problem.

Quantum computing is increasingly attracting interest from industry and scientific groups that use high-performance computing for their applications. These pilot users of quantum computing are primarily interested in testing whether available quantum computing technologies are suitable today or in the

foreseeable future for solving problems relevant to them. An important question to be answered is, which of these problems can be formulated such that a quantum or a hybrid quantum-classical algorithm can be developed to solve them.

How Pupils Solved the n-Queens Problem on a D-Wave System
René Grünbauer (Gymnasium Regensburger Domspatzen)

Eight chess queens must be placed on a chessboard so that no two queens threaten each other. The general form of this well-known problem (n queens on an n × n board) was solves on a D-Wave quantum annealer by three schoolboys (age 14, 15 and 16) from the high school of the "Regensburger Domspatzen". Their project won the first price at a regional youth science competition (Jugend forscht 2019).

As the supervisor of the three boys I will explain what it took to teach the boys how to use a D-Wave quantum annealer, how much knowledge of quantum physics was necessary and what the pupils had to know about formulating a mathematical puzzle as a quadratic unconstrained binary optimization (QUBO) problem.

With this knowledge my students could develop an energy function for the n-queens problem on their own. Their function returns a value for every constellation from zero up to n × n queens on a n × n chessboard. The global minima of this function represent the solutions of the n-queens problem. Once the problem was well-matched to the hard-wired design of the quantum annealer chip of a D-Wave 2000Q system, the n-queen problem was solved really, really fast...

Details of the solving algorithm and how to determine the energy function for this problem will be explained by my students live on stage.

Solving the Binary Paintshop Problem with the Quantum Approximate Optimisation Algorithm
Martin Leib (Volkswagen, Data:Lab)

We investigate the application of a novel heuristic algorithm for combinatorial optimization with noisy intermediate scale quantum (NISQ) processors, the Quantum Approximate Optimization Algorithm, (QAOA) to solve an industry relevant problem, the binary paint shop problem. In the binary painthop problem we strive to minimize the number of color changes that are necessary to color a given sequence of cars, because color changes in the paintshop require expensive cleaning procedures. Every car has to be painted twice with two different colors, however there is no predefined sequence the colors have to be applied. This problem is known to be NP-hard, i.e. it is intractable to find the optimal solution, and additionally APX-hard, i.e. it is even difficult to find a good approximation to the problem. We present classically simulated results of the application of QAOA on the binary paintshop problem. QAOA is a

hybrid quantum algorithm for NISQ devices that in its original version consists of a parametrized circuit that is optimized with an outer learning loop. We show how to come up with good parameters for the circuits with little to no prior execution of the parametrized circuit on the quantum processor.

Airbus Application Activies for Quantum Computing
Gerd Buettner (Airbus Operations GmbH)

Airbus start Quantum Computing activities already some yeras ago. Lessons learned from past projects and an overview on activities and ongoing projects. Finish with an Outlook of future Airbus Quantum Computing Challenges.

Room: Panorama 2
11:00 am - 12:30 pm

Life Sciences: How HPC is Changing the Medical Field

In Situ Data Analytics for Next Generation Molecular Dynamics Workflows
Michela Taufer (The University of Tennessee Knoxville)

Molecular dynamics (MD) simulations studying the classical time evolution of a molecular system at atomic resolution are widely recognized in the fields of chemistry, material sciences, molecular biology, and drug design; these simulations are one of the most common simulations on supercomputers. Next-generation supercomputers will have dramatically higher performance than do current systems, generating more data that needs to be analyzed (i.e., in terms of number and length of MD trajectories). The coordination of data generation and analysis cannot rely on manual, centralized approaches as it is predominately done today.

In this talk we discuss how the combination of machine learning and data analytics algorithms, workflow management methods, and high performance computing systems can transition the runtime analysis of larger and larger MD trajectories towards the exascale era. We demonstrate our approach on three case studies: protein-ligand docking simulations, protein folding simulations, and analytics of protein functions depending on proteins' three-dimensional structures. We show how, by mapping individual substructures to metadata, frame by frame at runtime, we can study the conformational dynamics of proteins in situ. The ensemble of metadata can be used for automatic, strategic analysis and steering of MD simulations within a trajectory or across trajectories, without manually identify those portions of trajectories in which rare events take place or critical conformational features are embedded.

HPC and Medical Treatment: a View from the Front Lines

Craig stewart (Indiana University, Pervasive Technology Institute)

This talk will describe how HPC is changing medical service delivery and biomedical research today with a view from the front lines: the view from the patient, the practitioner, and the researcher. Cancer treatment is changing so rapidly that treatments available to a patient with a particular cancer are changing - and improving quality of life and health outcomes - during the time a person is being treated. (The presenter is one example - he is being treated successfully for cancer with a personalized medicine approach, using monoclonal antibodies that were not available for treatment on the day he was diagnosed with cancer).

This discussion will start with an analysis of HPC in practical use guiding treatment for cancer. I will focus particularly on how HPC is being used in the newest developments in cancer research across the US - as the nature of cancer research and treatment change. One particular example that will be discussed is HPC in developing treatment for triple-negative breast cancer. The role of HPC in Alzheimer's research, and understanding basic brain function will be discussed.

This discussion will describe a mix of advances in software and software systems, personalized medicine, and strategies for rising use of HPC and cloud architectures.

The Role of High Performance Computing in Biomedicine

Peter V. Coveney (University College London, University of Amsterdam)

The era of personalised medicine offers at once a huge opportunity and a major challenge to computational science. The potential impact centres around our ability to marshal substantial quantities of patient data and to use them to perform predictive, mechanistic modelling and simulation in order to deliver therapies and to enhance clinical decision making, on time scales which are far shorter than those usually considered in the context of academic research and development activities. Secure access to personal data, as well as to powerful computational resources, is essential. I shall provide a couple of examples which illustrate the current state of the art. One addresses clinical decision support in the context of blood flow within neurovascular pathologies; the other is concerned with patient specific drug discovery and treatment. We shall discuss the underlying e-infrastructure requirements, including data, compute and networks, and reflect on the potential for cloud and other forms of e-infrastructure provision to meet the anticipated future demand for resources.

Room: Panorama 1

1:45 pm - 3:15 pm

Performance Tuning and Tools for HPC Systems

Lightweight Requirements Engineering for Exascale Co-design

Felix Wolf (TU Darmstadt)

Given the tremendous cost of an exascale system, its architecture must match the requirements of the applications it is supposed to run as precisely as possible. Conversely, applications must be designed such that building an appropriate system becomes feasible, motivating the idea of co-design. In this process, a fundamental aspect of the application requirements are the rates at which the demands for different resources grow as a code is scaled to a larger machine. However, if the anticipated scale exceeds the size of available platforms this demand can no longer be measured. This is clearly the case when designing an exascale system. Moreover, creating analytical models to predict these requirements is often too laborious—especially when the number and complexity of target applications is high. In this paper, we show how automated performance modeling can be used to quickly predict application requirements for varying scales and problem sizes.

Monitoring Inter-Thread Communication

Didem Unat (Koç University)

In a multicore environment, inter-thread communication can provide valuable insights about the application performance. Literature detecting inter-thread communication either employ hardware simulators or binary instrumentation. Those techniques bring both space and time overhead, which makes them impractical to use on real-life applications. Instead, we take a completely different approach that leverages hardware performance counters and debug registers to detect communication volume between threads. In this talk, we present the details of our approach along with some experimental results.

Analysing and Tuning the Performance of Graph Processing Algorithms: a Statistical Modeling Approach

Ana Lucia Varbanescu (University of Amsterdam)

Large-scale and complex graph processing applications form a challenging domain for high-performance computing. Despite graph processing algorithms being considered parallelism-unfriendly, the use of parallel architectures like multi-core CPUs and GPUs have proven revolutionary for these applications. However, analysing and modeling the performance of these algorithms on parallel platforms remains a challenge: the tight dependencies between platform, algorithm, and dataset are proven difficult to analytically determine, model, and feed back into the algorithm design.

In this work, we present a comprehensive framework for graph processing performance analysis, and further demonstrate its use for performance modeling and tuning. Our solution is based on a statistical approach, and combines efficient model training with accurate predictions. We are further able to use these predictions to improve algorithm execution. Finally, we present the performance analysis and tuning of two case-studies (BFS and PageRank), and demonstrate how to use performance modeling to obtain better implementations, which clearly outperform state-of-the-art implementations.

Room: Panorama 2
1:45 pm - 3:15 pm

Extreme-Scale/Exascale Applications China, Japan, World

Scaling Implicit Solvers to Millions of Cores

Chao Yang (Peking University)

The rapid development of supercomputers and the growing needs of extreme-scale applications pose grand challenges in the design of highly efficient and scalable parallel algorithms. It is of crucial importance to adapt the parallel algorithm with the architectural features so that the potential of the supercomputers can be fully unleashed at the extreme scale. In this talk, I will summarize our recent efforts on designing implicit solvers that aim to take full advantage of state-of-the-art many-core based heterogeneous supercomputers. A series of examples on both Tianhe-2 and Sunway TaihuLight are presented to show how high performance can be achieved in emergning benchmarks such as HPCG and HPGMG and challenging applications such as nonhydrostatic atmospheric dynamics and gaseous wave detonations.

Parallel Multigrid with Adaptive Multilevel hCGA on Manycore Clusters

Kengo Nakajima (University of Tokyo, Supercomputing Research Division, Information Technology Center; RIKEN R-CCS (Center for Computational Science))

A multigrid is a scalable multilevel method for solving linear equations and preconditioning Krylov iterative linear solvers, and is especially suitable for large-scale problems because of its scalable feature. The parallel multigrid method is expected to be one of the most powerful tools on exa-scale systems. In the previous work (K. Nakajima, IEEE ICPADS 2014), we have already developed an FVM code for 3D Groundwater Flow through Heterogenous Porous Media (pGW3D-FVM) with MGCG solvers (Multigrid Preconditioned Conjugate Gradient) using OpenMP/MPI with RCM (Reverse Cuthill-Mckee), and it is ready for exa-scale systems by hCGA (Hierarchical Coarse Grid Aggregation). hCGA provided significant improvement of performance (60% in weak scaling, 600% in strong scaling) for 3D FVM application on

4,096 nodes of Oakleaf-FX for problems with 1.8×10^10 DOF. Because the hCGA can only handle 2-hierarchica-levels, we are developing AM-hCGA (Adaptive Multilevel hCGA) for multiple hierarchical levels (more than three). In this presentation, we will present preliminary results of AM-hCGA on the Oakforest-PACS, Joint Center for Advanced High Performance Computing (JCAHPC), which consists of 8,208 nodes of Intel Xeon Phi (Knights Landing).

Simulation-Enabled Discoveries in Fluid Turbulence
Ravi Samtaney (KAUST)

Computation has emerged as the indispensable third leg of scientific discovery along with the traditional two branches of theory and experiment. In this talk we discuss discoveries that resulted from high-performance simulations of turbulent and magnetohydrodynamics (MHD) flows. We present results from DNS (direct numerical simulation) and LES (large-eddy simulation) of convective turbulence and wall-bounded turbulent flows. An open question in convective turbulence pertained to the scaling behavior of the energy spectrum. Our largest spectral simulation at a resolution of 40963 led to the conclusion that the energy spectrum follows the Kolmogorov scaling (k-5/3). An open question in wall-bounded turbulent flows is whether the mean velocity profile obeys a log-law or a power-law. Our LES results at extremely large Reynolds numbers (Re~1011) provide strong evidence that turbulence gravitates naturally towards the log-law scaling. Another interesting discovery is about the so-called “drag crisis”, i.e., the drag undergoes a drastic reduction at Re~300,000. Our LES have overturned the conventional wisdom that the drag crisis is due to the transition of the boundary layer from a laminar to a turbulent state. We believe these case studies amply demonstrate that simulation enabled discoveries are no longer a myth, and that computations are a legitimate tool to answer clearly posed questions in science and engineering.
Acknowledgement: The Cray XC40 Shaheen II at KAUST was used for all simulations reported. This research was partially supported under the KAUST Competitive Research Grant funds and baseline research funds of R. Samtaney.

Room: Panorama 1
4:00 pm - 5:00 pm

When is enough, enough? With so many Parallel Programming Technologies, is it Time to Focus on Consolidating them?

When is enough, enough? With so many Parallel Programming Technologies, is it Time to Focus on Consolidating them?
Hari Subramoni (The Ohio State University), Mirko Rahn (Fraunhofer ITWM), Rosa Badia (Barcelona Supercomputing Center), Bradford Chamberlain (Cray), Nick Brown (Edinburgh Parallel Computing

Centre (EPCC), The University of Edinburgh)

When it comes to parallel programming technologies most people in the HPC community agree that the most popular ones are not ideal, however, that's about all we can agree on! Whether it be classical HPC technologies such as MPI and OpenMP, those built on explicit parallel models such as OmpSs, Legion, GPI-Space, UPC++, Charm++, HPX, Chapel, and GASPI, those targeting accelerators such as OpenACC, OpenCL, CUDA, or domain specific languages, there are very many choices when it comes to writing parallel code. But all of these require significant investment from an application programmer, not just to learn but also risks associated in adoption for their application. So maybe it is unsurprising that, even though there are very many programming options, developers still frequently opt for the lowest common denominator of basic OpenMP or MPI v1. There is a saying, better the devil you know, and even though classical parallel technologies might not be perfect, at-least their ubiquity means that they are well supported, their future assured and programmers to some extent know what to expect. There is no single, silver bullet, technology, but whilst it can be argued a choice of parallel programming models is advantageous, crucially this approach spreads the community's effort out rather thinly. This panel will be focussed around the question of whether we should be looking more closely at consolidating and combining existing parallel programming technologies, standardisation to enable better interoperability and what sort of parallel programming technologies as a community we should be getting behind.

Room: Panorama 2
6:15 pm - 6:30 pm

Closing

Hans Meuer Award Finalists

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Monday, June 17th

Room: Panorama 1
4:00 pm - 6:00 pm

Research Paper (Award) Session 01

Session Description: The following awards will be given to outstanding research papers submitted to the conference: HANS MEUER AWARD The Hans Meuer Award honors the most outstanding research paper submitted to the conference's Research Papers Committee. This award has been introduced in the memory of the late Dr. Hans Meuer, general chair of the ISC conference from 1986 through 2014, and co-founder of the TOP500 project. From all submitted research papers, the Research Papers Committee will select the overall best paper for the award. GAUSS AWARD The GCS Award honors the most outstanding research paper submitted to the Research Papers Committee in the field of HPC. The GCS Award has been a key component of the conference each year since the foundation of the Gauss Centre for Supercomputing (GCS) in 2008. It is sponsored by GCS, an alliance of Germany's three national supercomputing centers — the High-Performance Computing Center Stuttgart (HLRS), Jülich Supercomputing Centre (JSC), and Leibniz Supercomputing Centre (LRZ).

Introduction Award Session
Yutong Lu, Carsten Trinitis

Hans Meuer Award Finalist 1: GPUMixer: Performance-Driven Floating-Point Tuning for GPU Scientific Applications
Ignacio Laguna (Lawerence Livermore National Laboratory)

We present GPUMixer, a tool to perform mixed-precision floating-point tuning on scientific GPU applications. While precision tuning techniques are available, they are designed for serial programs and are accuracy-driven, i.e., they consider configurations that satisfy accuracy constraints, but these

configurations may degrade performance. GPUMixer, in contrast, presents a performance-driven approach for tuning. We introduce a novel static analysis that finds Fast Imprecise Sets (FISets), sets of operations on low precision that minimize type conversions, which often yield performance speedups. To estimate the relative error introduced by GPU mixed-precision, we propose shadow computations analysis for GPUs, the first of this class for multi-threaded applications. GPUMixer obtains performance improvements of up to 46.4% of the ideal speedup in comparison to only 20.7% found by state-of-the-art methods.

Hans Meuer Award Finalist 2: Global Task Data Dependencies in PGAS Applications
Joseph Schuchart (Universität Stuttgart, Höchstleistungsrechenzentrum Stuttgart)

Recent years have seen the emergence of two independent programming models challenging the traditional two-tier combination of message passing and thread-level work-sharing: partitioned global address space (PGAS) and task-based concurrency. In the PGAS programming model, synchronization and communication between processes are decoupled, providing significant potential for reducing communication overhead. At the same time, task-based programming allows to exploit a large degree of shared-memory concurrency. The inherent lack of fine-grained synchronization in PGAS can be addressed through fine-grained task synchronization across process boundaries. In this work, we propose the use of task data dependencies describing the data-flow in the global address space to synchronize the execution of tasks created in parallel on multiple processes. We present a description of the global data dependencies, describe the necessary interactions between the distributed scheduler instances required to handle them, and discuss our implementation in the context of the DASH C++ PGAS framework. We evaluate our approach using the Blocked Cholesky Factorization and the LULESH proxy app, demonstrating the feasibility and scalability of our approach.

GCS Award Winning Paper: End-to-end Resilience for HPC Applications
Frank Mueller (NCSU)

A plethora of resilience techniques have been investigated ranging from checkpoint/restart over redundancy to algorithm-based fault tolerance. Each technique works well for a different subset of application kernels, and depending on the kernel, has different overheads, resource requirements, and fault masking capabilities. If, however, such techniques are combined and they interact across kernels, new vulnerability windows are created. This work contributes the idea of end-to-end resilience by protecting windows of vulnerability between kernels guarded by different resilience techniques. It introduces the live vulnerability factor (LVF), a new metric that quantifies any lack of end-to-end protection for a given data structure. The work further promotes end-to-end application protection across kernels via a pragma-based specification for diverse resilience schemes with minimal programming effort. This lifts the data protection burden from application programmers allowing them to focus solely on algorithms and performance while resilience is specified and subsequently embedded into the code

through the compiler/library and supported by the runtime system. Two case studies demonstrate that end-to-end resilience meshes well with different execution paradigms and assess its overhead and effectiveness for different codes. In experiments with case studies and benchmarks, end-to-end resilience has an overhead over kernel-specific resilience of less than 3% on average and increases protection against bit flips by a factor of three to four.

Tuesday, June 18th

Room: Panorama 2
5:00 pm - 5:15 pm

Hans Meuer Award Ceremony

Session Description: The Hans Meuer Award honors the most outstanding research paper submitted to the conference's Research Papers Committee. This award has been introduced in the memory of the late Dr. Hans Meuer, general chair of the ISC conference from 1986 through 2014, and co-founder of the TOP500 project.

HPC in Asia

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Tuesday, June 18th

Room: Areal
11:00 am - 4:45 pm

Research Posters + PhD Forum Posters + HPC in Asia Posters

Session Description: For a complete list of the Research Posters on display at ISC 2019, please refer to the
overview
of the Research Posters Session on Tuesday, June 18. For a complete list of the PhD Forum Posters on display at ISC 2019, please refer to the
overview
of the PhD Forum Posters Session on Monday, June 17. For a complete list of the HPC in Asia Posters on display at ISC 2019, please refer to the
overview
of the HPC in Asia Posters Session on Wednesday, June 19. For a complete list of the Woman in HPC Posters on display at ISC 2019, please refer to the
overview
of the Woman in HPC Posters on Tuesday, June 18.

Wednesday, June 19th

Room: Analog 1, 2
8:30 am - 10:10 am

HPC in Asia Session 01: Status report from nine countries

Welcome Address & Overview
Kengo Nakajima (The University of Tokyo, Supercomputing Division Information Technology Center)

Status Report from Thailand

Piyawut Srichaikul ((Thailand) National Electronics and Computer TEchnology Center, NSTDA Supercomputer Center)

Status Report from Taiwan

Weicheng Huang (National Center for High-performance Computing)

Status Report from Singapore

Stephen Wong (National Supercomputing Centre (NSCC) Singapore)

This talk will highlight the recent developments in Singapore in the HPC arena. The key area discussed will be Singapore's plans to build a supercomputing infrastructure to support the nation's R&D activities in the academia and the industry.

Status Report from Saudi Arabia

David Keyes (KAUST)

Two Saudi Arabian institutions rely heavily on supercomputing: Saudi Aramco, the world's most valuable company, and KAUST, one of the world's newest universities. For both, the predominant applications are in simulation; we mention as well initial forays into scientific machine learning. We describe the evolving field of play, the drivers, and issues of connectivity, facilities, and workforce development. KAUST was founded in 2009 with research thrusts in energy, environment, food, and water for a sustainable planet, and supporting thrusts in core capabilities (modeling, simulation, and analytics). It has operated a Top 20 supercomputer, used by both itself and Saudi Aramco, for most of its ten years, and with 46% of the faculty engaged on it, it could be the most computationally intensive university on the planet on a per faculty basis.

Status Report from Qatar

Othmane Bouhali (Texas A&M University at Qatar)

Status Report from Korea
Taeyoung Hong (KISTI)

Status Report from Japan
Satoshi Matsuoka (RIKEN Center for Computational Science, Tokyo Institute of Technology)

Status Report from China
Depei Qian (Beihang University, Sun Yat-sen University)

Status Report from Australia
Allan W. Williams (Australian Natioanl University, National Computational Infrastructure)

Questions & Answers

Room: Areal
8:30 am - 5:00 pm

Research Posters + PhD Forum Posters + HPC in Asia Posters

Session Description: For a complete list of the Research Posters on display at ISC 2019, please refer to the

overview
of the Research Posters Session on Tuesday, June 18. For a complete list of the PhD Forum Posters on display at ISC 2019, please refer to the
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overview
of the Woman in HPC Posters on Tuesday, June 18.

Room: Analog 1, 2
10:10 am - 11:00 am

HPC in Asia Poster Session

(RP01) CPU Water Cooling Temperature Effects on the Performance and Energy Consumption
Jorji Nonaka (RIKEN R-CCS)

Energy efficiency has become one of the critical element for data center operation. Recently, hot water cooling technology is famous as an approach to reduce power consumption for cooling and to improve PUE (Power Usage Effectiveness). In the hot water cooling, since the cooling water temperature is higher than the outside air temperature, a part or all of the exhaust heat is naturally cooled by the outside air. Therefore, it is possible to reduce power consumption for cooling. On the other hand, recent Intel architecture based CPU has a mechanism to automatically lower the clock frequency when it gets hot to prevent thermal runaway and failure. And in general, the power consumption of the CPU increases as the CPU temperature becomes higher as the leakage current increases. To fairly evaluate the effectiveness of the hot water cooling from the viewpoint of energy efficiency, the effect of increasing the power consumption of the CPU, the impact on degrading the performance and the effect of lowering the power consumption for cooling is needed to take into consideration. In this poster, we try to evaluate the impact of increasing the power consumption of the CPU and the impact on degrading the performance qualitatively and systematically by investigating the change in sustained performance and power consumption when CPU cooling water temperature changes.

(RP03) Design of an FPGA-based Matrix Multiplier with Task Parallelism

Yiyu Tan (RIKEN Center for Computational Science)

Matrix multiplication is one of the fundamental building blocks of linear algebra. It requires computer systems have huge computing capability as problem size is increased. In this research, an FPGA-based matrix multiplier with task parallelism is designed and implemented by using the FPGA board DE5a-NET. The matrix multiplier is based on the systolic array architecture with 10 × 16 processing elements, all modules except the data loading modules are autorun to hide computation overhead, and data of matrix A are shifted from left to right while data of matrix B are moved from top to bottom in the systolic array to reuse data. After implementation by using FPGA, the proposed matrix multiplier utilizes more DSP blocks and achieves much higher clock frequency over the Intel's OpenCL example with data parallelism on FPGA. When data are single-precision floating-points, the proposed matrix multiplier averagely achieves about 785 GFLOPs in computation throughput and 81 GFLOPs/W in energy efficiency. Compared with the Intel's OpenCL example with data parallelism on FPGA, software simulations based on the Intel MKL and OpenBLAS libraries, the proposed matrix multiplier averagely outperforms by 3.2 times, 1.3 times, and 1.6 times in computation throughput, and by 3.4 times, 12.7 times, and 14.6 times in energy efficiency, respectively, even if the fabrication technology of FPGA is 20 nm while it is 14 nm in CPU.

(RP04) Distributed Deep Learning with FPGA Ring Allreduce

Kenji Tanaka (NTT Corporation, NTT Device Technology Laboratories)

Among various methods for efficient distributed Deep Learning (DL), the top three state-of-the-art ImageNet/ResNet-50 training were achieved by utilizing a distributed data-parallel DL with Ring Allreduce or 2D-Torus Allreduce. However, it is difficult to apply them at large scale because latency is accumulated at each node due to data moving to GPU or CPU for Reduce processes. Our solution is to use In-Network Computing to handle data reduction while it is being transferred in the network. Since the conventional In-Network Computing system can apply to only hierarchical Allreduce, in this work, we propose a new In-Network Computing system that can support Ring Allreduce. In order to minimize communication overhead, we apply layer-based computing/communication overlap and optimize it for our proposed In-Network Computing system. We also propose a highly productive software stack consisting of a DL framework and heterogeneous device control languages. The evaluation results show that we can reduce the communication overhead by 84.27% at a batch size of 32 without any accuracy degradation. Moreover, the total learning time can be reduced by 7% when using 4 nodes learning system. It is confirmed that our system can significantly reduce the communication overhead without deteriorating accuracy when applying to a large-scale distributed DL with a large communication load. Although the current top data is 2-D Torus Allreduce using ASIC in domain specific architecture, the result shows that the communication overhead is shorter by applying the proposed system, which indicates the possibility of In-Network Computing.

(RP10) High-Performance Computing of Thin QR Decomposition on Parallel Systems

Takeshi Terao (Shibaura Institute of Technology)

This poster aims to propose the preconditioned Cholesky QR algorithms for thin QR decomposition (also called economy size QR decomposition). CholeskyQR is known as a fast algorithm employed for thin QR decomposition, and CholeskyQR2 is recently proposed for improving the orthogonality of a Q-factor computed by CholeskyQR. Although such Cholesky QR algorithms can efficiently be implemented in high-performance computing environments, they are not applicable for ill-conditioned matrices, as compared to the Householder QR and the Gram-Schmidt algorithms. To address this problem, we propose two algorithms named LU-Cholesky QR and Robust Cholesky QR. On LU-Chlesky QR, we apply the concept of LU decomposition to the Cholesky QR algorithms, i.e., the idea is to use LU-factors of a given matrix as preconditioning before applying Cholesky decomposition. Robust Cholesky QR uses a part of Cholesky factor for constructing the preconditioner when Cholesky decomposition breaks down. The feature of Robust Cholesky QR is its adaptiveness for difficulty of problems. In fact, the cost for the preconditioning in Robust Cholesky QR can be omitted if a given matrix is moderately well-conditioned. Numerical examples provided in this poster illustrate the efficiency of the proposed algorithms in parallel computing on distributed memory computers.

(RP12) A Container-Based Approach to HPC Cloud

Guohua Li (KISTI/Korea National Supercomputing Center)

Recently, the VM-based HPC service has been provided in the cloud environment to satisfy portability, flexibility, scalability, and reduction of deployment costs in the HPC field. However, performance issues and workload management issues due to the limitations of VM are reducing the resource utilization of HPC users. Therefore, we aim to provide a lightweight container-based cloud environment to HPC users. This container-based approach consists of two main components: the image management system and the workload management system. We have designed and implemented the system workflow and architecture considering ease of use and efficiency of management. The results have been obtained by comparing network performance, MPI performance and a simple machine learning code – MNIST between bare-metal and container-based (both in Docker and Singularity) environments.

(RP13) An Application Parameter Search Method Based on the Binary Search Algorithm for Performance Tuning

Takumi Kishitani (Tohoku University)

Because of the complexity of modern computer systems, such as many-core processors and heterogeneous memory systems, performance tuning is necessary to achieve high performance in scientific and engineering applications. The performance tuning needs to adjust many tuning parameters provided by systems and applications. As the number of parameters increases, the number of their combinations to be searched increases. Moreover, the execution times of simulation applications become

long because of their problem sizes and resolutions to solve. This situation causes an increase in a time for selecting an appropriate combination of the tuning parameters. This poster proposes the method to reduce the time to search the appropriate combination of the tuning parameters by the method based on the binary search algorithm. The proposed method select the appropriate application parameters such as inputs and iteration counts whiling keep the feature of the application. By executing the application with the smaller resolution and iteration counts than with original ones, each execution time for parameter tuning can be reduced. The evaluation results by using the tsunami simulation on Intel Xeon Phi Knights Landing show that the proposed method can select the most appropriate combination of the tuning parameters, and the parameter tuning time is reduced by 78.7% compared with the full search algorithm.

(RP15) Easy-to-use and Secure Web Command Line Interface for Heterogeneous Resources on Artificial Intelligence Platform

Rongqiang Cao (Computer Network Information Center, Chinese Academy of Sciences)

Command Line Interface (CLI) is still an important way to interact with computing resources today, but it is not easy for users to configure and access remote computing resources regarding network security and polices. Further, it is much difficult for users to learn many commands and adopt them to manage applications, tasks and data on different computing resources. We proposed event-based web services to smooth the sharp learning curve of CLI and will finally provide easy-to-use web CLI (WebCLI) services for users on our AI platform [http://ai.sccas.cn]. In WebCLI, command recommendation service is designed to help user write and complete a complicated command according to personal history commands, user's behaviors, the global data and different preference configurations. Command combination service is designed to accept characters from a terminal running in browser and generate an entire command to shield syntax differences caused by various job management systems in heterogeneous resources. Security and risk service is designed to check whether each command gets permission to execute based on multi-levels white lists and black lists. It also present warnings to users if any command especially on delete will cause unrecoverable outcomes. Based on Eclipse Vert.x, a prototype was implemented to verify usability and availability. In a browser, a user can login CLI to access heterogeneous resources, query history commands in detail, and track each actions of a workflow. In future, we will continue to extend the prototype system to a productive system on the AI platform.

(RP16) Power Prediction with Probabilistic Topic Modeling for HPC

Shigeto Suzuki (FUJITSU LABORATORIES LTD.)

Hundreds-MW power will be required for exa-scale supercomputer in 2023, so the power consumption becomes a critical factor for the next-generation systems. A power-aware scheduling with job power prediction is a key technology to achieve energy-efficient operation and high system utilization. Recently, there is a significant number of researches about predicting job power from job entries such as user-id, number of nodes by using machine learning. One challenge for making these approaches into realization

is tough tuning of weights for each job entries because the weights of each job entries is different for each site. In this work, we develop the novel two-step power prediction model combining topic model and probabilistic model. The model can predict each job power from submitted job entries without manual tuning of the weight. First, all the job entries of a target job are fed to the trained topic model to derive 10 candidate jobs from the past job database. Then, the probabilistic model selects one job from the 10 candidates that has the highest probability of success and uses its power as a prediction of the target job. The probabilistic model has automatically trained how to weight these job entries based on the relationship between the past entries and the power prediction results. We demonstrated 3-month power prediction of K computer. The average relative error with 18 % was achieved for the total job power prediction. The proposed two-step scheme has better accuracy of 3.1% in comparison with one-step, topic model only, scheme.

(RP18) Real-Time Fire Detection Using CUDA

Manal Jalloul (American University of Beirut)

In this research, a high-resolution real-time fire detection system was implemented. NVIDIA CUDA framework was used to parallelize a serial version that was implemented using OpenCV. The algorithm relies on color thresholding with other de-noising image processing techniques applied to track the fire. Both implementations of the fire detection algorithm were compared, and the reported results show that the parallel implementation achieved a 60% speedup over the serial version.

(RP20) Development of Training Environment for Deep Learning With Medical Images on Supercomputer System Based on Asynchronous Parallel Bayesian Optimization

Yukihiro Nomura (The University of Tokyo Hospital)

Recently, deep learning has been exploited in the field of medical image analysis. However, deep learning requires large amounts of computational power, and optimization of numerous hyper-parameters largely affects the performance of deep learning. If a framework for training deep learning with hyper-parameter optimization on a supercomputer system can be realized, it is expected to accelerate training of deep learning with medical images. In this study, we described our novel environment for training deep learning with medical images on the Reedbush-H supercomputer system based on asynchronous parallel Bayesian optimization (BO). Our training environment was composed of an automated hyper-parameter tuning module based on BO and a job submission module based on Xcrypt, which is a job level parallel script language based on Perl. The training jobs using the hyper-parameters generated by the hyper-parameter tuning module were alternately executed at the compute nodes. In training of deep learning using our framework, the hyper-parameters were chosen by BO so as to maximize the value of evaluation criteria in validation. We targeted an automated detection of lung nodule in chest computed tomography images based on a 3D U-Net. In this case, we selected 11 types of hyper-parameters. The tuning performance with sequential BO was superior to that with asynchronous parallel BO. When the

number of workers was eight or less, the tuning performance with asynchronous parallel BO was superior to that with random search. The constructed environment enabled to efficiently train deep learning with hyper-parameter tuning on the Reedbush-H supercomputer system.

(RP23) A Skewed Multi-Bank Cache for Vector Processors

Hikaru Takayashiki (Tohoku University)

Vector supercomputers are widely used in scientific and engineering applications that require a high memory bandwidth. Recently, the key component of the vector supercomputers, a vector processor, has adopted a multi-core architecture that plays an important role for improving computing performance. On the other hand, improvement of the memory bandwidth is limited due to memory technology trends. Hence, the vector processor employs multi-bank cache memories in order to obtain high memory data transfer capability. It is expected that these trends continue, and more cores and caches with more banks will be used even in future vector processors. However, cache configurations suitable for vector processors are not clear in the case of many cores and many cache banks. The preliminary evaluation using a simulator shows that a vector processor with many cores and many banks causes a lot of conflict misses in the stencil kernel. Therefore, this poster proposes a skewed multi-bank cache for the many-core vector processors that enables to suppress conflict misses with a low associativity. This poster examines odd-multiplier displacement hashing as a hash function for skewing and SRRIP as a cache replacement policy. The evaluation results show that, by adopting the skewed multi-bank cache for a many-core vector processor, almost ideal hit ratio can be obtained in the stencil kernel.

(RP27) Memory First : A Performance Tuning Strategy Focusing on Memory Access Patterns

Naoki Ebata (Tohoku University)

As many scientific applications are memory-bound, a key to achieving high sustained performance on a modern HPC system is to fully exploit the system's memory bandwidth. Indeed, the sustained memory bandwidth of an application could be much lower than the theoretical peak bandwidth of the system for various reasons due to underlying memory architectures. For example, a certain memory access pattern may cause frequent access conflicts at memory channels and/or banks, and thus lead to a longer access latency. This poster hence discusses a memory-centric performance tuning strategy, Memory First. Usually, a whole application is first written and then optimized for a particular system, often resulting in major code modifications for memory-aware tuning. On the other hand, in the Memory First strategy, memory access patterns capable of achieving high sustained memory bandwidths on a target system are first investigated. Then, unlike the conventional strategy, a tiny benchmark code achieving a high sustained memory bandwidth is developed, while keeping a target application's behavior in mind. Finally, the code is modified to work as the target application. While application coding is well established in matured application areas such as CFD, memory-aware tuning is likely to become more painful in practice. This is because the latter has to be developed for every new architecture in a try-and-error

fashion. Therefore, giving a higher priority to memory-aware tuning can result in a lower tuning cost in modern HPC systems with advanced memory technologies, such as NEC SX-Aurora TSUBASA.

(RP28) Performance Tuning of Deep Learning Framework Chainer on the K Computer.
Akiyoshi Kuroda (RIKEN, R-CCS)

Recently the applications and research of machine learning by deep learning has become popular using GPU. However, it seems possible to do many calculations using CPUs of massively parallel computers. Here, we introduce some performance tuning procedures for Chainer, which is a representative framework for utilization of machine learning on the K computer. Chainer expresses the hierarchical structure of deep learning using Python, and all calculations can be realized using numPy without special libraries. By optimizing floating point underflow exception when building Python, elapsed time was improved to 1/3.39. Moreover, by replacing the SSL2 gemm library called by Python with the thread-parallel version, section elapsed time was improved to 1/4.54, the total elapsed time was improved to 1/1.15, and the performance efficiency was improved about 47.0%. Many of the cost was the calculation of the square root and the arithmetic when the filter was updated and activation functions. These operations are not optimized when calculated using numPy and are particularly slow on the K computer. By replacing the kernel with software pipelining and SIMD optimization by Fortran library, the kernel elapsed time was improved to 1/11.08 and total elapsed time was improved to 1/16.23. There are some limitations on the use of Chainer on the K computer. However, it can be said that deep learning calculation became possible on the K computer and the Post-K computer using these tuning effect and CPU parallel version Chainer.

Room: Analog 1, 2
11:00 am - 12:30 pm

HPC in Asia Session 02

Update of the Post-K and Japanese HPCI
Mitsuhisa Sato (RIKEN CCS, RIKEN)

We have been developing the Japanese flagship supercomputer, post-K system. The system development is now moving to production phase, and the early access program will be scheduled in the next year. The HPCI is a shared computational environment which connects the K computer and other major supercomputers as well as storages of universities and research institutions in Japan via high speed networks. The HPCI will be updated by the post-K and other new universities supercomputers. In this talk, the details of the post-K system and the update of the HPCI with the related advanced software

and applications projects will be presented.

Scalable Graph Traversal on Sunway TaihuLight with Ten Million Cores
Jidong Zhai (Tsinghua University)

Interest has recently grown in efficiently analyzing unstructured data such as social network graphs and protein structures. A fundamental graph algorithm for doing such task is the Breadth-First Search (BFS) algorithm, the foundation for many other important graph algorithms such as calculating the shortest path or finding the maximum flow in graphs. In this talk, I will share our experience of designing and implementing the BFS algorithm on Sunway TaihuLight, a newly released machine with 40,960 nodes and 10.6 million accelerator cores. It tops the Top500 list of June 2016 with a 93.01 petaflops Linpack performance. Designed for extremely large-scale computation and power efficiency, processors on Sunway TaihuLight employ a unique heterogeneous many-core architecture and memory hierarchy. With its extremely large size, the machine provides both opportunities and challenges for implementing high-performance irregular algorithms, such as BFS. We propose several techniques, including pipelined module mapping, contention-free data shuffling, and group-based message batching, to address the challenges of efficiently utilizing the features of this large scale heterogeneous machine. We ultimately achieved 23755.7 giga-traversed edges per second (GTEPS), which is the best among heterogeneous machines and the second overall in the Graph500s June 2016 list.

Digital Annealer: A Dedicated System for Quadratic Unconstrained Binary Optimization
Hirotaka Tamura (Fujitsu Laboratories LTD.)

We have proposed the Digital Annealer (DA) as an option for improving computing performance after the end of Moore's law. The DA is a dedicated system for Quadratic Unconstrained Binary Optimization (QUBO), where a quadratic function of binary bits is minimized without constraint. A chip named the Digital Annealing Unit (DAU) is used as a hardware optimization engine in the DA. The current generation of the DAU can handle QUBO, in which up to 8k bits are fully connected through 16- to 64-bit weights. The DAU uses Markov Chain Monte Carlo (MCMC) as a basic search mechanism, accelerated by the use of hardware parallelism that achieves near rejection-free MCMC operation, where the state changes without a rejection for each Metropolis iteration. As an optimizer, the DAU utilizes Parallel Tempering in addition to ordinary Simulated Annealing, thus providing better solutions and ease of annealing schedule adjustment. In this talk, the design concept of the DA, the principle of the speeding-up method by parallel operation, and the benchmark results showing the effect of this method will be presented.

HPC in Asia Poster Awarding & Closing
Kengo Nakajima

Industrial Day

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Tuesday, June 18th

Room: Panorama 1
8:30 am - 10:00 am

Industrial Market for HPC

HPC Applications @ BASF
Stephan Schenk (BASF SE)

The talk will give an overview of Digitalization activities at BASF with a focus on the application of High Performance Computing in R&D. It will be shown how HPC supports research projects for a broad variety of applications.

A Global Study: Best Practices in Partnerships between HPC Centers and Industry
Steve Conway (Hyperion Research)

This study, conducted for the National Center for Supercomputing Applications (NCSA) at the University of Illinois at Urbana-Champaign, distilled best practices from interviews with HPC centers and industrial users of the centers around the world, in the hope that this information will be useful to all parties involved today in partnerships like these, or considering such involvement. A finding Hyperion Research considers especially important is that where collaborations exist, both the HPC centers and industrial partners typically said that they benefit from the relationships: ▪ The industrial partners reported benefits including increased competitiveness, new discoveries and insights, and faster development of products and services, among other advantages. ▪ The surveyed HPC centers reported benefits including unexpected new pathways for science, increased motivation and retention of their scientific and computational personnel, and additional revenue for reinvestment in the centers.

Room: Panorama 1
11:00 am - 12:30 pm

HPC Applications in Industry

HPC Applications @ Airbus

Sebastian Lange (Airbus)

The world of HPC in industry is very different from the academic scope of supercomputing. Besides the much smaller scales, also self-developed parallel codes are quite rare. This talk will give an overview of HPC-Applications at Airbus, especially in the Satellite business. Different approaches will be discussed, as well as the gap between recent development of the supercomputing hardware and the todays needs of industry.

HPC-as-a-Service for Innovation and Research Applications

Stéphane Jay (IFPEN)

This talk will concern an HPC-as –a-Service solution designed to help industrial users get access to state-of-the-art models for high fidelity flow resolution. The application will be introduced with a particular focus on the HPC requirements and illustrations of possible usage in the field of high efficiency thermal automotive engines design will be presented.

Bringing HPC Clusters to the Cloud with Infrastructure as Code

Jochen Heil (GNS Systems GmbH)

Bringing HPC Clusters to the Cloud with Infrastructure as Code

Cloud and High Performance Computing used to be completely separate realms. This is changing – finally. But some important questions remain:

- Are the hyperscalers' present offerings actually suitable for industrial HPC workloads?

- Can cloud infrastructure deployment be simple, easily repeatable, and vendor agnostic?

We address scenarios arising from industrial CAE workloads, introduce matching HPC cluster architectures, and show how HashiCorp's "Packer" and "Terraform" Infrastructure as Code (IaC) tools can be used to implement them in a vendor-agnostic way.

Room: Panorama 1
1:45 pm - 3:15 pm

Synergies of AI/ML and HPC in Industry

Massively Parallel Virtual Testing of Safety-Relevant Driving Systems

Alexander Thieß (Spicetech GmbH)

Testing and validation are cost-intense parts in the automotive development process already today. On top of that, the emerging development of autonomous driving vehicles is demanding scenario and validation spaces being by orders of magnitude more complex than nowadays tasks and moreover not well-defined. E.g. the correct classification of objects depends on a vast variety of attributes, such as shape, color, texture, reflectivity, road infrastructure, ambient weather conditions are only one example. How to truly validate such complex systems in such complex variety of conditions? For many of such safety-critical systems this task has to be mastered by means of virtual validation and cover at least millions of virtual tests. Obviously, this tasks these have to be executed as fast as possible to enable a continuous development process for the development of autonomous systems.

Using high-performance computing (HPC) as well as artificial intelligence (AI) and machine learning (ML) algorithms we developed the framework VALICY, which is designed to master virtual validation tasks of high complexity. Systems under validation, e.g. decision functions in car control units or sensor functions of end-users, have been successfully integrated into the framework, and by that, validated on HPC systems on thousands of processors guaranteeing e.g. overnight feedback even for 15-20 dimensional variational test spaces. To exemplify the application of the framework, validation scenarios for camera-based object detection and classification functions will be shown and discussed in this talk.

Autonomous Driving Development Platform for Data Driven Engineering and Testing

Valerio Zanetti-Ueberwasser (T-Systems), Andreas Findling (Cray Computer Deutschland GmbH)

This talk provides insights into autonomous driving development platforms. It covers the whole process to support the development of intelligent functionalities for autonomous driving. T-Systems/Cray will present its portfolio of platform technologies and services to support this ecosystem. Platforms for developing AI based safety critical devices and functions need specific software and hardware optimizations. Because of the shift from code to data driven engineering and the increasing need for virtual and physical tests, co-design of workloads and underlying platform becomes a necessity. Short development cycles reduce space for any kind of data movements or overheads. The capability to instantly analyze data on the edge or near a testbed becomes more important. Large test data sets from distributed field tests must be analyzed in a geo-federated way. Not only bridging geo-distance but also system borders becomes crucial to efficiently run simulations without duplicating data and orchestration code. Re-simulation has to

be seamless from numerical to physical simulations on HIL's and testbeds. Orchestration, workload management and APIs provide the basis for such an integrated development and simulation platform. Seamlessly embedding development and test pipelines by optimizing data flows reduces time and cost to get results.

Accelerating Fluid Flow Prediction 1000X with Deep Learning - A Case Study
Wolfgang Gentzsch (UberCloud)

Solving fluid flow problems using computational fluid dynamics (CFD, here OpenFOAM) is demanding both in terms of computing power and simulation time, and requires deep expertise in CFD. In this project, together with partners Renumics and Advania Data Centers, an Artificial Neural Network (ANN) has been applied to predicting the fluid flow given only the shape of the object that is to be simulated. The goal is to apply an ANN to solve fluid flow problems to significantly decrease time-to-solution while preserving much of the accuracy of a traditional CFD solver. Creating a large number of simulation samples is paramount to let the neural network learn the dependencies between simulated design and the flow field around it.

Synergies of AI/ML and HPC in Industry
Brendan McGinty (National Center for Supercomputing Applications (NCSA), University of Illinois at Urbana-Champaign), Seid Koric (National Center for Supercomputing Applications (NCSA), University of Illinois at Urbana-Champaign)

The rise of the fourth paradigm of science, which is data-driven discovery, has been lately enabled by our ability to collect and analyze "big data" on HPC.

In our talk, after brief introduction to NCSA Industry - the largest industrial HPC outreach in the world - we shall discuss examples of some recent advances in this field in terms of development and application of big data analytics and Artificial Intelligence in the various domains of industrial interest such as geospatial information systems (GIS), AI driven multiscale models in materials science and the convergence of CFD and AI in turbulence modeling.

Room: Panorama 1
3:45 pm - 4:45 pm

AI goes Mainstream - Who cares about HPC?

Session Description: After a full day with talks around the industrial use of HPC and AI and how they may play together, we will try to take a look behind the mechanisms that drive not only the development of these technologies but also the needs of industry in this context. Our panelists will share their view on how HPC and AI will grow together (will they?) and how the role of HPC probably changes when AI is the new mainstream hot topic. In our discussion we will determine the status quo and try to develop a perspective for the coming developments.

AI goes Mainstream - Who cares about HPC?

Wolfgang Gentzsch (UberCloud), Stephan Schenk (BASF SE), Valerio Zanetti-Überwasser (T-Systems), Alexander Thieß (Spicetech GmbH), Andreas Wierse (SICOS BW GmbH)

After a full day with talks around the industrial use of HPC and AI and how they may play together, we will try to take a look behind the mechanisms that drive not only the development of these technologies but also the needs of industry in this context. Our panelists will share their view on how HPC and AI will grow together (will they?) and how the role of HPC probably changes when AI is the new mainstream hot topic. In our discussion we will determine the status quo and try to develop a perspective for the coming developments.

Keynote

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Monday, June 17th

Room: Panorama 2, 3
9:30 am - 10:30 am

ISC 2019 Conference Keynote

The Algorithms of Life - Scientific Computing for Systems Biology
Ivo Sbalzarini (TU Dresden, Faculty of Computer Science; MOSAIC Group, Center for Systems Biology Dresden)

Scientific high-performance computing is of rapidly growing importance and influence in the life sciences. Thanks to the increasing knowledge about the molecular foundations of life, recent advances in biomedical data science, and the availability of predictive biophysical theories that can be numerically simulated, mechanistic understanding of the emergence of life comes within reach. Computing is playing a pivotal and catalytic role in this scientific revolution, both as a tool of investigation and hypothesis testing, but also as a school of thought and systems model. This is because a developing tissue, embryo, or organ can itself be seen as a massively parallel distributed computing system that collectively self-organizes to bring about behavior we call life. In any multicellular organism, every cell constantly takes decisions about growth, division, and migration based on local information, with cells communicating with each other via chemical, mechanical, and electrical signals across length scales from nanometers to meters. Each cell can therefore be understood as a mechano-chemical processing element in a complexly interconnected million- or billion-core computing system. Mechanistically understanding and reprogramming this system is a grand challenge. While the “hardware” (proteins, lipids, etc.) and the “source code” (genetic code) are increasingly known, we known virtually nothing about the algorithms that this code implements on this hardware. Our vision is to contribute to this challenge by developing computational methods and software systems for high-performance data analysis, inference, and numerical simulation of computer models of biological tissues, incorporating the known biochemistry and biophysics in 3D-space and time, in order to understand biological processes on an algorithmic basis. This ranges from real-time approaches to biomedical image analysis, to novel simulation languages for parallel high-performance computing, to virtual reality and machine learning for 3D microscopy and numerical simulations of coupled biochemical-biomechanical models. The cooperative, interdisciplinary effort to develop and advance our understanding of life using computational approaches not only places high-performance computing center stage, but also provides stimulating impulses for the future

development of this field.

Tuesday, June 18th

Room: Panorama 2
5:15 pm - 6:00 pm

Tuesday Keynote

HPC Beyond Moore's Law
John Shalf (Lawrence Berkeley National Laboratory)

Moore's Law is a techno-economic model that has enabled the Information Technology (IT) industry to nearly double the performance and functionality of digital electronics roughly every two years within a fixed cost, power and area. Within a decade, the technological underpinnings for the process Gordon Moore described will come to an end as lithography gets down to atomic scale. At that point, it will be feasible to create lithographically produced devices with characteristic dimensions in the 3nm5nm range. This range corresponds to a dozen or fewer Si atoms across critical device features and will therefore be a practical limit for controlling charge in a classical sense. The classical technological driver that has underpinned Moore's law for the past 50 years is already failing and is anticipated to flatten by 2025. This talk provides an updated view of what a 2021-2023 system might look like and the challenges ahead, based on our most recent understanding of technology roadmaps. It also will discuss the tapering of historical improvements in lithography, and how it affects options available to continue scaling of successors to the first exascale machine

Wednesday, June 19th

Room: Panorama 2
5:30 pm - 6:15 pm

Wednesday Keynote

HPC Achievement and Impact – 2019
Thomas Sterling (School of Informatics, Computing, and Engineering Indiana University)

It’s hard to believe, but it is quite possible that the first declaration of success in the quest for exaflops will be in less than two years. This 16th closing ISC Keynote will capture the final sprint to this self-declared milestone. And yet even as it is approached, so many other aspects of the HPC field are pushing for the dominance of center stage. Linpack endures. But a growing appreciation that Rmax is not the measure of all things is expressed by new driver applications such as various forms of Machine Learning and as quantum computing garners massive amounts of international funding in support of extreme (sometimes exponential) claims. But the community will argue when exascale is achieved until Rmax of 1 Exaflops is reached and verified. And then it may be wondered: “for what?”. Because progress in performance, energy efficiency, size, cost, and user productivity must be measurably pursued, there is no stopping unless we’re forced to. Has the field already been conceded to the Chinese? Is Japan right and the race is for Graph-500 and ML, not HPL. Is the European new energy for the hardware market share the next metric of accomplishment? Is this the next ARMs race? Ultimately, when does the entire concept of von Neumann cores become obsolete? Surely, we don’t want another Roadrunner or Aurora. This fast-paced presentation will punch through the barriers to progress. Is risk-adverse the riskiest strategy? Is past success the path to future failure? Let’s get at it!

Machine Learning Day

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Wednesday, June 19th

Room: Panorama 3
8:30 am - 10:00 am

AI4ALL, Keynotes #1 Machine Learning Day

Deep Learning Acceleration of Progress toward Delivery of Fusion Energy
William M. Tang (Princeton University, PPPL)

Accelerated progress in delivering accurate predictions in science and industry have been accomplished by engaging advanced statistical methods featuring machine/deep learning/artificial intelligence (ML/DL/AI). Associated techniques have enabled new avenues of data-driven discovery in key scientific applications areas such as the quest to deliver Fusion Energy – identified by the 2015 CNN “Moonshots for the 21st Century” televised series as one of 5 prominent grand challenges for the world today. An especially time-urgent and challenging problem facing the development of a fusion energy reactor is the need to reliably predict and avoid large-scale major disruptions in magnetically-confined tokamak systems such as the EUROFUSION Joint European Torus (JET) today and the burning plasma ITER device in the near future. Significantly improved methods of prediction with better than 95% predictive accuracy are required to provide sufficient advanced warning for disruption avoidance/mitigation strategies to be effectively applied before critical damage can be done to ITER -- a ground-breaking $25B international burning plasma experiment with the potential capability to exceed “breakeven” fusion power by a factor of 10 or more with “first plasma” targeted for 2026. This presentation will introduce high performance computing (HPC) relevant advances in the deployment of deep learning recurrent and convolutional neural networks in Princeton’s Deep Learning Code -- "FRNN” -- on top supercomputing systems worldwide that have accelerated progress in predicting tokamak disruptions with unprecedented accuracy and speed (Ref. “NATURE,” to be published, May 2019). Powerful current HPC systems engaged include SUMMIT in the US and ABCI in Japan.

Machine Learning for Systems
Azalia Mirhoseini (Google Brain)

I will present some of our recent work at the intersection of machine learning and systems. First, I discuss

our work on the sparsely-gated mixture of experts, a neural architecture that allows training models with 130B+ parameters (10x larger than any previous model) on datasets with 100B+ examples. This architecture uses an intelligent gating mechanism that routes input examples to a subset of the modules (“experts”) within the larger model. This model runs 2-3x faster than top-performing baselines and sets a new state of the art in machine translation and language modeling. Next, I discuss our work on deep reinforcement learning models that learn to do resource allocation, a combinatorial optimization problem that repeatedly appears in computer systems. Our method is end-to-end and abstracts away the complexity of the underlying optimization space; the RL agent learns the implicit tradeoffs between computation and communication of the underlying resources and optimizes the allocation using only the true reward function (e.g., the runtime of the generated allocation). The complexity of our search space is on the order of 9^80000, compared to 10^360 states for Go (solved by AlphaGo). Finally, I discuss our work on deep models that learn to find solutions for the classic problem of balanced graph partitioning with minimum edge cuts. Our method enables generalization; we can train models that produce performant partitions at inference time on unseen graphs. The generalization significantly speeds up the partitioning process over all existing baselines which solve the problem from scratch for each new graph.

Room: Panorama 3
11:00 am - 12:30 pm

AI4ALL, Machine Learning Day

Solving IO Bottlenecks for Deep Learning on Large Scale Brain Images
Lena Oden (Fernuniversität Hagen)

The use of Deep Learning methods has been identified as a key opportunity for enabling processing of extreme-scale scientific datasets. Facilitating processing of these datasets thus requires the ability to store petabytes of data as well as to access the data with very high bandwidth. Many HPC clusters still follow the Beowulf architecture , where the compute nodes have little or no storage space integrated within the node. For cytoarchitectonic brain mapping, for example, large scale images (up to 22GB per image) are accessed, which causes massive IO problems on our systems, due to very high bandwidth requirements and random, fine grand access patterns. Hierarchical storage architectures are a promising technology to allow faster access to frequently used data. However, the efficient use of staging layers is hard, since the faster layers usually have a lower capacity. We evaluate different methods of staging frequently used data in faster storage layers. Our staging techniques not only copy the data, but also perform transformations, which leads to better access patterns and reduces IO, which increases the total performance of our Deep Learning applications up to the factor of ten, compared to the original applications.

Deep Learning in Computer Assisted Medical Interventions

Tobias Ross (German Cancer Research Center, University of Heidelberg)

Surgical data science is a recent new research area that aims to observe all aspects of the patient treatment process in order to provide the right assistance a the right time. This talk will give a brief overview of the current work of the department "Computer Assisted Medical Interventions" of the German Cancer Research Center, how deep learning based methods could be applied to solve surgical data science challenges such as the visualization of hidden structures with insufficient or even no real training data.

Modelling The Language Of Life: From NLP to BioInformatics

Ahmed Elnaggar (Technische Universität München)

Natural language processing field has seen a remarkable breakthrough in 2018 in almost all public datasets by using the new era of context aware embedding, including different models like: ULMFiT, ELMo, OpenAI GPT and BERT. The advantages of these language models are that they can effectively capture the semantic, syntactic and grammar meaning of characters, words sentences from large unlabelled datasets. Which, can be used later to provide better representation for sentences for many NLP tasks. Unfortunately, these models have not been leveraged in other similar fields like Bioinformatics. This talk will give an overview of the current transfer learning context aware embedding models in NLP, and how it was applied in the Bioinformatics field to boost the performance on many use-cases. Furthermore, it will cover the current HPC limitation that makes it difficult to apply these techniques in the Bioinformatics field.

RAPIDS: Data Science on GPUs

Christoph Angerer (NVIDIA)

GPUs and GPU platforms have been responsible for the dramatic advancement of deep learning and other neural net methods in the past several years. At the same time, traditional machine learning workloads, which comprise the majority of business use cases, continue to be written in Python with heavy reliance on a combination of single-threaded tools (e.g., Pandas and Scikit-Learn) or large, multi-CPU distributed solutions (e.g., Spark and PySpark). RAPIDS, developed by a consortium of companies and available as open source code, allows for moving the vast majority of machine learning workloads from a CPU environment to GPUs. This allows for a substantial speed up, particularly on large data sets, and affords rapid, interactive work that previously was cumbersome to code or very slow to execute. By keeping all data analytics tasks on the GPU and minimizing redundant I/O, data scientists are enabled to model their data quickly and frequently, affording a higher degree of experimentation and more effective model generation. Further, keeping all of this in compatible formats allows quick movement from feature

extraction, graph representation, graph analytic, enrichment back to the original data, and visualization of results. RAPIDS has a mission to build a platform that allows data scientist to explore data, train machine learning algorithms, and build applications while primarily staying on the GPU and GPU platforms.

Room: Panorama 3
1:45 pm - 3:15 pm

HPC4AI, Machine Learning Day

Building Machine Learning Systems at Scale - a Case Study

Janis Keuper (Fraunhofer ITWM)

In this talk, we will review current approaches to build large scalable machine learning (deep learning) systems for academic research and industrial development in the context of autonomous driving applications. We will discuss recent approaches in hardware architecture and software stacks, as well as open problems.

Optimizing and Benchmarking Large-Scale Deep Learning

Torsten Hoefler (ETH Zurich)

We introduce schemes to optimize communication in deep learning workloads. For this, we use properties of the standard SGD algorithm that allows us to delay the sending of some parts of the gradient updates. Our implementation SparCML speeds up practical workloads significantly. We then discuss Deep500: the first customizable benchmarking infrastructure that enables fair comparison of the plethora of deep learning frameworks, algorithms, libraries, and techniques. The key idea behind Deep500 is its modular design, where deep learning is factorized into four distinct levels: operators, network processing, training, and distributed training. Our evaluation illustrates that Deep500 is customizable (enables combining and benchmarking different deep learning codes) and fair (uses carefully selected metrics). Moreover, Deep500 is fast (incurs negligible overheads), verifiable (offers infrastructure to analyze correctness), and reproducible. Finally, as the first distributed and reproducible benchmarking system for deep learning, Deep500 provides software infrastructure to utilize the most powerful supercomputers for extreme-scale workloads.

Accelerating Deep Learning via Adaptive Deep Reuse

Xipeng Shen (North Carolina State University (NCSU))

One of the key road blocks in practical adoptions of Deep Neural Networks (DNN) is the long training process of DNN models. This talk presents adaptive deep reuse, a novel optimization to the-state-of-the-art training methods of DNN. Adaptive deep reuse offers a creative way to efficiently and effectively identify unnecessary computations in DNN training on the fly. By avoiding these computations, it cuts the training time of DNN by 69% without sacrificing accuracy. The method is fully automatic and ready to adopt, requiring neither manual code changes nor extra computing resource. It offers a promising way to substantially reduce both the time and the cost in the development of AI products.

Room: Panorama 3
4:00 pm - 5:00 pm

AI and Security, Keynote #2 Machine Learning Day

AI and Security in Three Acts
Ian Molloy (IBM Research)

Machine learning and artificial intelligence are incredibly powerful tools that have become pervasive in our lives. Large datasets combined with massive computing power has resulted in models whose accuracy excedes that of humans at narrowly scoped tasks, such as computer vision, speech recognition, and natural language processing. From the earliest Bayesian spam filters to the latest deep learning models, researchers have tried to adopt the machine learning tools to improve security and privacy. However, the adoption of machine learning is not without its consequences and we must face the sobering truth about technology: any tool or technology can be the target of adversaries or used for nefarious objectives. AI is no different. In this talk I'll expand on three themes at the intersection of AI and security: the use of AI in security; attacking AI; and the weaponization of AI.

Cognitive Simulation: Intersection of Large Scale Machine Learning and Scientific Computing
Brian C. Van Essen (Lawrence Livermore National Laboratory (LLNL))

Large-scale scientific endeavors often focus on improving predictive capabilities by challenging theory-driven simulations with experimental data. We'll describe our work at LLNL using advances in deep learning, computational workflows, and computer architectures to develop a cognitive simulation framework that is able to interface large scale machine learning with scientific simulation. We will present how this framework in the context of Inertial Confinement Fusion (ICF) simulation, focusing one the challenges of scalable deep learning.

We'll discuss necessary advances in machine learning architectures and methods to handle the

challenges of ICF science, including rich, multimodal data (images, scalars, time series) and strong nonlinearities. These include advances in the scalability of our deep learning toolkit LBANN, an optimized asynchronous, GPU-Aware communication library, and a state-of-the-art scientific workflows. We'll also how the combination of high-performance NVLINK and the rich GPU architecture of Sierra enables us to train neural networks efficiently and begin to develop learned predictive models based on a massive data set.

Panel

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Tuesday, June 18th

Room: Panorama 1
3:45 pm - 4:45 pm

AI goes Mainstream - Who cares about HPC?

Session Description: After a full day with talks around the industrial use of HPC and AI and how they may play together, we will try to take a look behind the mechanisms that drive not only the development of these technologies but also the needs of industry in this context. Our panelists will share their view on how HPC and AI will grow together (will they?) and how the role of HPC probably changes when AI is the new mainstream hot topic. In our discussion we will determine the status quo and try to develop a perspective for the coming developments.

AI goes Mainstream - Who cares about HPC?
Wolfgang Gentzsch (UberCloud), Stephan Schenk (BASF SE), Valerio Zanetti-Überwasser (T-Systems), Alexander Thieß (Spicetech GmbH), Andreas Wierse (SICOS BW GmbH)

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Room: Panorama 2
3:45 pm - 4:45 pm

High Performance Computing in 2029 or The Cambrian Explosion in Computing in the 2020s

High Performance Computing in 2029 or The Cambrian Explosion in Computing in the 2020s
John Shalf (Lawrence Berkeley National Laboratory), Kristel Michielsen (Jülich Supercomputing Centre (JSC), RWTH Aachen University), Yutong Lu (National Supercomputer Center in Guangzhou), Kengo Nakajima (University of Tokyo, Supercomputing Research Division, Information Technology Center; RIKEN R-CCS), Jack Dongarra (University of Tennessee, Oak Ridge National Laboratory)

The next decade promises to be one of the most exciting yet in the further evolution of computing. There are a number of developments that will change how we will compute in 10 years: the foreseeable end of Moore's law will lead to the exploration of new architectures and the introduction of new technologies in HPC; the rapid progress in machine learning in the last decade has led to a refocus of HPC towards large scale data analysis and machine learning; the feasibility of quantum computing has led to the introduction of new paradigms for scientific computing; meanwhile 30 billion IOT devices will push advances in energy efficient computing and bring an avalanche of data. I would like to compare the situation to a Cambrian explosion: the change in computing environment has helped creating a wide and complex variety of "organisms" that will compete for survival in the next decade. The HPC community will have to deal with this complexity and extreme heterogeneity, and decide what ideas and technologies will be the survivors. In this panel, I will ask several worldwide HPC experts to make their predictions for 2030.

Wednesday, June 19th

Room: Panorama 1
4:00 pm - 5:00 pm

When is enough, enough? With so many Parallel Programming Technologies, is it Time to Focus on Consolidating them?

When is enough, enough? With so many Parallel Programming Technologies, is it Time to Focus on Consolidating them?
Hari Subramoni (The Ohio State University), Mirko Rahn (Fraunhofer ITWM), Rosa Badia (Barcelona Supercomputing Center), Bradford Chamberlain (Cray), Nick Brown (Edinburgh Parallel Computing Centre (EPCC), The University of Edinburgh)

When it comes to parallel programming technologies most people in the HPC community agree that the most popular ones are not ideal, however, that's about all we can agree on! Whether it be classical HPC technologies such as MPI and OpenMP, those built on explicit parallel models such as OmpSs, Legion, GPI-Space, UPC++, Charm++, HPX, Chapel, and GASPI, those targeting accelerators such as OpenACC, OpenCL, CUDA, or domain specific languages, there are very many choices when it comes to

writing parallel code. But all of these require significant investment from an application programmer, not just to learn but also risks associated in adoption for their application. So maybe it is unsurprising that, even though there are very many programming options, developers still frequently opt for the lowest common denominator of basic OpenMP or MPI v1. There is a saying, better the devil you know, and even though classical parallel technologies might not be perfect, at-least their ubiquity means that they are well supported, their future assured and programmers to some extent know what to expect. There is no single, silver bullet, technology, but whilst it can be argued a choice of parallel programming models is advantageous, crucially this approach spreads the community's effort out rather thinly. This panel will be focussed around the question of whether we should be looking more closely at consolidating and combining existing parallel programming technologies, standardisation to enable better interoperability and what sort of parallel programming technologies as a community we should be getting behind.

PhD Forum

(back to top)

Monday, June 17th

Room: Analog 1, 2
1:00 pm - 3:00 pm

PhD Forum

Welcome & Introduction
Florina Ciorba (University of Basel), Martin Schulz (Technical University of Munich)

(PhD01) A Fast Multipole Method for Training Neural Networks
Severin Reiz (Technische Universität München)

We propose a fast multipole method for the fast approximation and factorization of the Gauss-Newton Hessian for fully-connected multilayer perceptron and convolutional neural networks. We use a block-low rank approximation scheme that is inspired by methods for N-body problems in computational physics. In addition, we propose precomputation and sampling algorithms that reduce the complexity of the overall scheme. For a net with N weights, an average layer dimension d, and batch size n, the Gauss-Newton Hessian requires O(N 2 n) work and O(N 2) memory. By introducing a controllable approximation error, our method requires only O(dnN) work and O(N (n + r_o)) memory, where r o is the rank of the off-diagonal blocks of the Gauss-Newton Hessian. After construction, the cost of factorization of the regularized Gauss-Newton Hessian is O(N r_o^2), which results in an improvement of several orders of magnitude compared to the standard O(N^3) complexity for factorization of dense matrices of this size. If a global low-rank approximation of the Gauss-Newton Hessian is used, then we can construct an approximation and a factorization in O(N r 2) work and O(N r) memory. Our method becomes preferable when r_o

(PhD02) Scaling Stencil Computation on OpenPOWER Near-Memory Computing Architecture
Gagandeep Singh (TU Eindhoven, IBM Research - Zurich)

The traditional processor-centric approach of computation is based on moving data through a memory hierarchy into compute units. These memory units themselves are a passive component. This processor-centric approach takes advantage of data locality, in space and time, to hide the latency and energy overhead associated with data movement. However, modern HPC workloads such as graph processing and neural networks have a random-access behavior, leading to a poor locality that greatly reduces the advantage of a processor-centric approach.

With recent advances in memory architectures, we are witnessing a paradigm shift towards a data-centric approach, where data plays a central role instead of computing. This data-centric approach consists of placing compute units close to the memory to reduce unnecessary data movement, which is referred to as near memory computing (NMC). Conceptually this approach can be applied to any level or type of memory to improve the overall system performance. However, to establish NMC as a viable solution for current HPC applications, several key challenges need to be addressed, including system integration, architectural design space exploration, data mapping, cache coherency, and virtual memory support

We have developed an NMC performance prediction framework using ensemble learning that combines hardware parameters and application-specific characteristics to provide performance estimates for previously unseen applications. This framework can provide rapid exploration compared to a state-of-the-art NMC simulator. Our current focus is on intranode scaling for weather forecasting application on POWER9 and near-memory accelerators via high bandwidth OpenCAPI interface.

(PhD03) Design of Robust Scheduling Methodologies in High Performance Computing
Ali Mohammed (University of Basel)

Scientific applications are often irregular and characterized by large computationally-intensive parallel loops. The performance of scientific applications on high performance computing (HPC) systems may degrade due to load imbalance. Load imbalance may be caused by irregular computational load per loop iteration or irregular and unpredictable computing system characteristics. Dynamic loop scheduling (DLS) techniques improve the performance of computationally-intensive scientific applications by balancing the load during their execution. A number of dynamic loop scheduling (DLS) techniques have been proposed between the late 1980s and early 2000s and efficiently used in scientific applications. HPC systems have significantly advanced in recent decades and are continuing to grow in terms of computing power and memory. State-of-the-art HPC systems have several million processing cores and approximately 1 Petabyte of system memory. However, achieving a balanced load execution of scientific applications on such systems is challenging due to systems heterogeneity, unpredictable performance variations, perturbations, and faults. My Ph.D. aims to improve the performance of computationally-intensive scientific applications on HPC systems via robust load balancing under unpredictable application and system characteristics.

Given the significant advancement of HPC systems, the computing systems on which DLS techniques

have initially been tested and validated are no longer available. Therefore, this work is concerned with the minimization of the sources of uncertainty in the implementation of DLS techniques to avoid unnecessary influences on the performance of scientific applications. It is essential to ensure that the DLS techniques employed in scientific applications today adhere to their original design goals and specifications and attain trust in the implementation of DLS techniques in today's studies. To achieve this goal, verification of DLS techniques implementation via the reproduction of selected experiments [1] was performed via simulative and native experimentation.

Simulation alleviates a large number of exploratory native experiments required to optimize applications performance, which may not always be feasible or practical due to associated time and costs. Bridging the native and simulative executions of parallel applications are needed for attaining trustworthiness in simulation results. To this end, a methodology for bridging the native and simulative executions of parallel applications on HPC systems is devised in this work. The experiments presented in this poster confirm that the simulation reproduces the performance achieved on the past computing platform and accurately predicts the performance achieved on the present computing platform. The performance reproduction and prediction confirm that the present implementation of the DLS techniques considered both, in simulation and natively, adheres to their original description.

Using the above simulation methodology, trusted simulation of application performance was leveraged to achieve a balanced execution under perturbations via simulated assisted scheduling (SimAS). SimAS is a new control-theoretic inspired approach that predicts and selects DLS techniques that improve the performance under certain execution scenarios. The performance results confirm that the SimAS-based DLS selection delivered improved application performance in most experiments.

[1] S. Flynn Hummel, E. Schonberg, and L. E. Flynn, "Factoring: A method for scheduling parallel loops," Communications of the ACM, vol. 35, no. 8, pp. 90–101, 1992.

(PhD04) Multilevel Scheduling of Computations in Large-Scale Parallel Computing Systems

Ahmed Eleliemy (University of Basel)

Modern high performance computing (HPC) systems exhibit rapid growth in size, both "horizontally" in the number of nodes, as well as "vertically" in the number of cores per node. As such, they offer additional levels of hardware parallelism. Each such level requires and employs algorithms for appropriately scheduling the computational work at the respective level. Understanding this relation is important for improving the performance of scientific applications, that are scheduled and executed in batches on HPC systems. Understanding the relation between different levels of scheduling offers several opportunities to enhance application execution times and resource utilization as well. This Ph.D. work focuses on two scheduling levels: batch and application level scheduling. Using simulations and native experimentation, we try to offer any an answer to the following research question: Given massive parallelism, at multiple levels, and of diverse forms and granularities, how can it be exposed, expressed, and exploited such that

execution times are reduced, performance targets are achieved, and acceptable efficiency is maintained?

(PhD05) Virtual Reality In Situ Visualization with Interactive Steering for Numerical Simulations

Aryaman Gupta (Technische Universität Dresden; Max Planck Institute of Molecular Cell Biology and Genetics, Dresden)

Recent trends in high-performance computing have witnessed a disproportionate increase in computational throughput over I/O bandwidth to the disk. File I/O has thus become a bottleneck for scientific simulations, which generate large amounts of data. In-situ processing, where visualization or analysis run in parallel with simulation, has emerged as a viable solution as it allows the user to select regions of interest to be captured and written to the disk. It also enables steering of simulations.

While in situ visualization has received much research interest, it has not yet been achieved in Virtual Reality (VR) for large simulations. VR, offering immersive 3D visualization and real-time interactivity, has gained vast popularity in scientific visualization, including for the posthoc visualization of simulations. However, VR involves frequent viewpoint changes due to the user's head and body movements, and requires data to be rendered at high frame rates and low latency, otherwise the user may get sick or lose immersion. The results of large simulations are difficult to render in situ under such constraints.

The primary objective of this thesis is to develop a system that performs, and more generally, algorithms that enable, immersive in-situ visualization and steering of numerical simulations. More specifically, it is our objective to build from the ground up an architecture that optimizes frame rates and latency for in situ rendering, leveraging the power of modern high-performance computers. Immersive visualization has been shown to improve perception of space and geometry, and we believe in situ visualization in VR would significantly aid scientific discovery in complex three-dimensional simulations. We aim to further enhance the user's immersiveness through the use of Natural User Interface (NUI) based steering of simulations, e.g., the induction of boundary conditions in a fluid simulation through hand gestures. NUIs, interfaces based on body pose and gaze, have been shown to help scientists better understand data.

As part of our effort to build such an architecture, we have developed an open source parallel VR rendering library, which performs both volume and mesh rendering. It uses the high-performance Vulkan API for rendering, and therefore has the potential to harness the power of modern GPUs better than several prevalent in situ solutions, such as Paraview Catalyst and VisIt Libsim. We also develop and maintain an open source library for scalable numerical simulations. It performs dynamic load balancing and is capable of running on accelerators (GPUs).

We intend to implement a tightly coupled linking of the two libraries to minimize the cost of data transfer, with simulation and rendering taking place on the same cluster and, wherever possible, on the same nodes within the cluster. One of the core algorithmic issues we will be addressing is novel-view synthesis of volumetric data, to ensure that latency requirements are met when the user's head position changes.

Another challenge will be the optimal redistribution of simulation data for rendering when not all nodes in the cluster have a GPU. Further, we will investigate NUI based steering of scientific simulations.

(PhD06) Modeling Performance for Reconfigurable Computing with Structured Parallelism
Pascal Jungblut (Ludwig Maximilian University Munich (LMU))

The research examines how reconfigurable computing can be integrated in the context of structured parallelism.

Algorithmic skeletons have been proposed to decouple the semantics of an algorithm from its implementation. They allow a programmer to specify the algorithm in an abstract and concise way without hardware-dependent instructions. A runtime then uses the description in form of skeletons to use the provided hardware parallelism. One source of hardware parallelism are reconfigurable devices, such as FPGAs. They can offer speedups or energy savings compared to CPUs and GPUs but require additional configuration-phases, some even allow partial reconfiguration.

There are a some challenges when it comes to the integration of FPGAs. 1. The runtime for high-level codes on FPGAs is hard to estimate. One solution could be to assume the worst-case memory-bound performance. 2. Partial reconfiguration adds complexity that needs to be accounted for by the cost model. 3. When the CPU and the FPGA share the same connection to the memory, they inevitably influence each others execution, adding more complexity to consider.

Research questions are the following: - Given a composition of algorithmic skeletons, how can the execution be mapped to the hardware, especially if CPUs and FPGAs are available at the same time. - Does the memory bottleneck leave useful HPC applications where FPGAs should be used with high-level tools when targeting performance? - What is a cost model for offloading to reconfigurable devices in a high-level and possibly distributed programming context?

The implementation is build around an already existing C++ PGAS library. It used C++17 ranges to describe the algorithmic skeletons.

(PhD07) Parallel-In-Time Dynamo Simulations
Andrew T. Clarke (University of Leeds)

Objectives: Investigate suitability of parallel in time methods to speed up dynamo simulations. Explore performance of parareal algorithm when applied to kinematic dynamos. Compare performance of parareal with performance of PFASST when applied to kinematic dynamos. Explore performance of parareal and PFASST when applied to fully coupled magnetohydrodynamic simulations.

Early results: A combined space-time parallelisation using Parareal was found to deliver substantial speedup beyond the saturation point of purely spatial parallelisation. Speed up of over 300 found using 1600 processors, with efficiency of ~0.16.

Description of Work: The precise mechanisms responsible for the natural dynamos in the Earth and Sun are still not fully understood. Numerical simulations of natural dynamos are extremely computationally intensive, and are carried out in parameter regimes many orders of magnitude away from real conditions.

Parallelization in space is a common strategy to speed up simulations on high performance computers, but eventually hits a scaling limit because of increasing overheads from communication.. Additional directions of parallelization are desirable to utilise the high number of processor cores now available in current and future massively parallel high-performance computing systems.

Parallel-in-time methods can deliver speed up in addition to that offered by spatial partitioning but have not yet been applied to dynamo simulations. My research investigates the feasibility of using the parallel-in-time algorithm Parareal to speed up initial value problem simulations of the kinematic dynamo, using the open source Dedalus spectral solver.

I have provided the first demonstration first demonstration that parallel-in-time methods can deliver speed up for the kinematic dynamo problem beyond the saturation point of spatial parallelization over a wide range of magnetic Reynolds numbers.

My poster will present an implementation of Parareal in the open source Python based Dedalus spectral solver. The code makes use of FFTW and MPI libraries for efficient parallel communications, with the mpi4py python library used to implement the Parareal algorithm, to run fully parallel in time and space simulations. The coarse solver is generated by coarsening in both spatial and time coordinates.

Both the time independent Roberts and time dependent Galloway-Proctor 2.5D dynamos are investigated over a range of magnetic Reynolds numbers.

Speed ups beyond those possible from spatial parallelisation are found in both cases. Results for the Galloway-Proctor flow are promising, with Parareal efficiency found to be close to 0.3. Roberts flow results are less efficient, but Parareal still shows speed up over spatial parallelisation alone. Parallel in space and time speed ups of ~300 were found for 1600 cores for the Galloway-Proctor flow, with total parallel efficiency of ~0.16

My results indicate that parallel in time methods are very promising for simulation of geo- and astro-dynamos and could allow investigation of parameter regimes closer to reality than have been hitherto possible.

Future work planned includes investigation of the method for non-linear MHD problems, and a

comparison of Parareal with alternative parallel-in-time algorithm PFASST.

(PhD08) Petalisp - Towards Fully Dynamic Program Optimization
Marco Heisig (FAU Erlangen-Nürnberg)

We present a new technique for parallel programming, where computation is expressed by assembling inherently parallel data flow graphs at run time and by submitting them to an extremely fast evaluator. In doing so, we unlock a lot of potential for automatic parallelization and obtain a programming model that is elegant and productive. The downside of this approach is the added run time overhead of assembling, analyzing, optimizing and scheduling data flow graphs.

We provide a practical and mature implementation of this technique with the Common Lisp library Petalisp. Our early results are promising and show that Petalisp programs can often outperform equivalent NumPy code and are slowly getting competitive even to optimized C++ code.

(PhD09) In-Situ Simulation Data Compression for Climate Domain
Anastasiia Novikova (Fraunhofer Institute for Computer Graphics Research IGD-Rostock, Hamburg Universität)

The need for storing of climate simulation data has been underlined by exploring of climate change. A climate model is a very complex multi-component system, which is ordinarily represented as multidimensional arrays of numbers with type of floating-point and contain a specific climate elements with such atmospheric parameters as temperature, humidity, precipitation, wind speed and power, and other. Usually dimensions of datasets are longitude, latitude, height and time. The amount of the data is growing exponentially, mostly at 40% to 60% year. Compression costs time for decoding and encoding data, but it reduces resource usage, data storage space and transmission capacity (throughput). This poster represents first results and methodology for the PhD work on data compression for climate domain. It consists of such sections: motivation of the work on data compression for this field, goals, methodology, an overview of the most popular algorithms, and first evaluation results (SCIL as HDF5 filter with other filters). Impact of SCIL usage on overall application performance will be studied.

PhD Forum Poster Session

ISC 2019 PhD Forum Award Ceremony

Room: Foyers
1:00 pm - 6:00 pm

PhD Forum Posters

(PhD01) A Fast Multipole Method for Training Neural Networks

Severin Reiz (Technische Universität München)

We propose a fast multipole method for the fast approximation and factorization of the Gauss-Newton Hessian for fully-connected multilayer perceptron and convolutional neural networks. We use a block-low rank approximation scheme that is inspired by methods for N-body problems in computational physics. In addition, we propose precomputation and sampling algorithms that reduce the complexity of the overall scheme. For a net with N weights, an average layer dimension d, and batch size n, the Gauss-Newton Hessian requires O(N 2 n) work and O(N 2) memory. By introducing a controllable approximation error, our method requires only O(dnN) work and O(N (n + r_o)) memory, where r o is the rank of the off-diagonal blocks of the Gauss-Newton Hessian. After construction, the cost of factorization of the regularized Gauss-Newton Hessian is O(N r_o^2), which results in an improvement of several orders of magnitude compared to the standard O(N^3) complexity for factorization of dense matrices of this size. If a global low-rank approximation of the Gauss-Newton Hessian is used, then we can construct an approximation and a factorization in O(N r 2) work and O(N r) memory. Our method becomes preferable when r_o

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approach, where data plays a central role instead of computing. This data-centric approach consists of placing compute units close to the memory to reduce unnecessary data movement, which is referred to as near memory computing (NMC). Conceptually this approach can be applied to any level or type of memory to improve the overall system performance. However, to establish NMC as a viable solution for current HPC applications, several key challenges need to be addressed, including system integration, architectural design space exploration, data mapping, cache coherency, and virtual memory support

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Simulation alleviates a large number of exploratory native experiments required to optimize applications performance, which may not always be feasible or practical due to associated time and costs. Bridging the native and simulative executions of parallel applications are needed for attaining trustworthiness in simulation results. To this end, a methodology for bridging the native and simulative executions of parallel applications on HPC systems is devised in this work. The experiments presented in this poster confirm that the simulation reproduces the performance achieved on the past computing platform and accurately predicts the performance achieved on the present computing platform. The performance reproduction and prediction confirm that the present implementation of the DLS techniques considered both, in simulation and natively, adheres to their original description.

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The primary objective of this thesis is to develop a system that performs, and more generally, algorithms that enable, immersive in-situ visualization and steering of numerical simulations. More specifically, it is our objective to build from the ground up an architecture that optimizes frame rates and latency for in situ rendering, leveraging the power of modern high-performance computers. Immersive visualization has been shown to improve perception of space and geometry, and we believe in situ visualization in VR would significantly aid scientific discovery in complex three-dimensional simulations. We aim to further enhance the user's immersiveness through the use of Natural User Interface (NUI) based steering of simulations, e.g., the induction of boundary conditions in a fluid simulation through hand gestures. NUIs, interfaces based on body pose and gaze, have been shown to help scientists better understand data.

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The implementation is build around an already existing C++ PGAS library. It used C++17 ranges to describe the algorithmic skeletons.

(PhD07) Parallel-In-Time Dynamo Simulations

Andrew T. Clarke (University of Leeds)

Objectives: Investigate suitability of parallel in time methods to speed up dynamo simulations. Explore performance of parareal algorithm when applied to kinematic dynamos. Compare performance of parareal with performance of PFASST when applied to kinematic dynamos. Explore performance of parareal and PFASST when applied to fully coupled magnetohydrodynamic simulations.

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My poster will present an implementation of Parareal in the open source Python based Dedalus spectral solver. The code makes use of FFTW and MPI libraries for efficient parallel communications, with the mpi4py python library used to implement the Parareal algorithm, to run fully parallel in time and space simulations. The coarse solver is generated by coarsening in both spatial and time coordinates.

Both the time independent Roberts and time dependent Galloway-Proctor 2.5D dynamos are investigated over a range of magnetic Reynolds numbers.

Speed ups beyond those possible from spatial parallelisation are found in both cases. Results for the Galloway-Proctor flow are promising, with Parareal efficiency found to be close to 0.3. Roberts flow results are less efficient, but Parareal still shows speed up over spatial parallelisation alone. Parallel in space and time speed ups of ~300 were found for 1600 cores for the Galloway-Proctor flow, with total parallel efficiency of ~0.16

My results indicate that parallel in time methods are very promising for simulation of geo- and astro-dynamos and could allow investigation of parameter regimes closer to reality than have been hitherto possible.

Future work planned includes investigation of the method for non-linear MHD problems, and a comparison of Parareal with alternative parallel-in-time algorithm PFASST.

(PhD08) Petalisp - Towards Fully Dynamic Program Optimization

Marco Heisig (FAU Erlangen-Nürnberg)

We present a new technique for parallel programming, where computation is expressed by assembling inherently parallel data flow graphs at run time and by submitting them to an extremely fast evaluator. In

doing so, we unlock a lot of potential for automatic parallelization and obtain a programming model that is elegant and productive. The downside of this approach is the added run time overhead of assembling, analyzing, optimizing and scheduling data flow graphs.

We provide a practical and mature implementation of this technique with the Common Lisp library Petalisp. Our early results are promising and show that Petalisp programs can often outperform equivalent NumPy code and are slowly getting competitive even to optimized C++ code.

(PhD09) In-Situ Simulation Data Compression for Climate Domain
Anastasiia Novikova (Fraunhofer Institute for Computer Graphics Research IGD-Rostock, Hamburg Universität)

The need for storing of climate simulation data has been underlined by exploring of climate change. A climate model is a very complex multi-component system, which is ordinarily represented as multidimensional arrays of numbers with type of floating-point and contain a specific climate elements with such atmospheric parameters as temperature, humidity, precipitation, wind speed and power, and other. Usually dimensions of datasets are longitude, latitude, height and time. The amount of the data is growing exponentially, mostly at 40% to 60% year. Compression costs time for decoding and encoding data, but it reduces resource usage, data storage space and transmission capacity (throughput). This poster represents first results and methodology for the PhD work on data compression for climate domain. It consists of such sections: motivation of the work on data compression for this field, goals, methodology, an overview of the most popular algorithms, and first evaluation results (SCIL as HDF5 filter with other filters). Impact of SCIL usage on overall application performance will be studied.

(PhD10) Smoothing Data Movement Between RAM and Storage for Reverse Time Migration
Tariq Alturkestani (KAUST)

Due to Moore's law, the performance of CPUs has been historically doubling every two years. However, storage systems have not been able to catch up in the same speed. I/O is considered a bottleneck for many critical simulations that rely on writing and reading intermediate results or snapshots during their computation. Reverse Time Migration (RTM), for example, is a seismic imaging method that compute high resolution image from seismic data, by propagating waves in 3D models. Based on an adjoint-state formulation, RTM requires combining at regular time steps a forward-propagated source wavefield with a back-propagated receiver wavefield. This process involves thus a first phase where the 3D simulation states, or snapshots, of the source wavefield are computed and saved at predetermined time steps. Then in a second phase, the receiver wavefield is computed and the imaging time steps, the source snapshots are retrieved and correlated with the receiver snapshots to update the final image. The time that is spent blocking for I/O during the two phases amount for about %68 of the entire execution time. Recent supercomputer architectures include several layers of storage from DRAM to BurstBuffer to disk, which

triggered the development of libraries implementing the checkpoint restart pattern, mainly for fault tolerance purpose. Utilization of these libraries for RTM, can improve the overall performances, mainly through asynchronous I/O accesses, which allow for a partial overlap with computations. However, most of these generic components are not optimal as they cannot benefit from the very regular access pattern in the RTM which allow for further performance gain through customized prefetching strategies. The system, Multilayered Buffer System (MLBS), proposed in this research, shows a general and versatile method for overlapping I/O with computation that helps to reduce the blocking time through asynchronous access and an RTM specific stage out and prefetching strategy, while minimizing the impact on the computational kernel. MLBS shows that coupling both storage and memory systems and using the knowledge of data access patterns can decrease the time spent blocking for I/O by more than %70 and thereby improving the entire execution time by 2.98X on regular storage and up to 3.95X on BurstBuffer.

Tuesday, June 18th

Room: Areal
11:00 am - 4:45 pm

Research Posters + PhD Forum Posters + HPC in Asia Posters

Session Description: For a complete list of the Research Posters on display at ISC 2019, please refer to the
overview
of the Research Posters Session on Tuesday, June 18. For a complete list of the PhD Forum Posters on display at ISC 2019, please refer to the
overview
of the PhD Forum Posters Session on Monday, June 17. For a complete list of the HPC in Asia Posters on display at ISC 2019, please refer to the
overview
of the HPC in Asia Posters Session on Wednesday, June 19. For a complete list of the Woman in HPC Posters on display at ISC 2019, please refer to the
overview
of the Woman in HPC Posters on Tuesday, June 18.

Wednesday, June 19th

Room: Areal

8:30 am - 5:00 pm

Research Posters + PhD Forum Posters + HPC in Asia Posters

Session Description: For a complete list of the Research Posters on display at ISC 2019, please refer to the
overview
of the Research Posters Session on Tuesday, June 18. For a complete list of the PhD Forum Posters on display at ISC 2019, please refer to the
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overview
of the Woman in HPC Posters on Tuesday, June 18.

Project Poster

(back to top)

Monday, June 17th

Room: Booth N-230
3:00 pm - 8:30 pm

Project Poster

Tuesday, June 18th

Room: Booth N-230
10:00 am - 6:00 pm

Project Poster

Room: Booth N-230
3:15 pm - 3:45 pm

Project Poster Presentation

(PP01): TaLPas: Task-Based Load Balancing and Auto-Tuning in Particle Simulations
Philipp Neumann (University Hamburg - Department of Informatics)

TaLPas will provide a solution to fast and robust simulation of many, inter-dependent particle systems in peta- and exascale supercomputing environments. This will be beneficial for a wide range of applications, including sampling in molecular dynamics (rare event sampling, determination of equations of state, etc.), uncertainty quantification (sensitivity investigation of parameters on actual simulation results), or parameter identification (identification of optimal parameter sets to fit numerical model and experiment).

For this purpose, TaLPas targets 1. the development of innovative auto-tuning based particle simulation software in form of an open-source library to leverage optimal node-level performance. This will guarantee an optimal time-to-solution for small- to mid-sized particle simulations, 2. the development of a

scalable workflow manager to optimally distribute inter-dependent particle simulation tasks on available HPC compute resources, 3. the investigation of performance prediction methods for particle simulations to support auto-tuning and to feed the workflow manager with accurate runtime predictions, 4. the integration of auto-tuning based particle simulation, scalable workflow manager and performance prediction, augmented by visualization of the sampling (parameter space exploration) and an approach to resilience. The latter will guarantee robustness at peta- and exascale.

Work presented at ISC will focus on steps 1-3. The integration of all components (step 4) is anticipated for the year 2019. To reach its goals, TaLPas bundles interdisciplinary expert knowledge on high-performance computing, visualization and resilience, performance modeling, and particle applications.

(PP02): The Virtual Institute for I/O and the IO-500
Julian Kunkel (University of Reading)

The research community in high-performance computing is organized loosely. There are many distinct resources such as homepages of research groups and benchmarks. The Virtual Institute for I/O aims to provide a hub for the community and particularly newcomers to find relevant information in many directions. It hosts the comprehensive data center list (CDCL). Similarly to the top500, it contains information about supercomputers and their storage systems.

I/O benchmarking, particularly, the intercomparison of measured performance between sites is tricky as there are more hardware components involved and configurations to take into account. Therefore, together with the community, we standardized an HPC I/O benchmark, the IO-500benchmark, for which the first list had been released during supercomputing in Nov. 2017. Such a benchmark is also useful to assess the impact of system issues like the Meltdown and Spectre* bugs.

This poster introduces the Virtual Institute for I/O, the high-performance storage list and the effort for the IO-500 which are unfunded community projects.

(PP03): NeIC presents Nordic Project Highlights: Nordic Resource Exchange & Highly-Available Storage Within Nordic LHC Tier-1
Michaela Barth (NeIC, NordForsk; PDC-HPC, KTH Royal Institute of Technology)

Through the Nordic e-Infrastructure Collaboration (NeIC) together the Nordic countries are tackling e-infrastructure challenges beyond singular national capabilities. Specific aspects of two current NeIC projects are highlighted on this poster.

Dellingr, NeIC's cross-border resource sharing project, contributes towards establishing a framework for resource sharing across the Nordics. Based on the experience of the first pilot the intented improved

resource access process is presented. Allocations will use billing units (BU) as a common currency and the Waldur cloud brokerage framework (https://share.neic.no) will be the central tool used throughout the whole process starting from resource application, over usage tracking to linking to resulting publications. https://dellingr.neic.no/apply/

Within the context of the Nordic Large Hadron Collider (LHC) Computing Tier-1 the effective high-availability routines since 2016 are presented. Conceived in 2002 as a one-of-a-kind facility unifying six academic computing centres in four different countries, the Nordic Tier-1 can now look back on more than 13 years of successful operations with an excellent track record on reliability and availability. Using the High-Availability (HA) features within dCache, ucarpd for automatic IP fail-over, HAProxy for load balancing and Ganeti as well as repmgr for managing VMs and HA PostgreSQL, no downtimes have to be scheduled for regular Linux security updates or dCache upgrades and no restrictions for the perceived user experience apply.

(PP04): The HPC PowerStack: A Community-Driven Collaboration Towards an Energy Efficient Software Stack

Siddhartha Jana (Energy Efficient HPC Working Group, Intel Corporation)

While there exist several standalone efforts that attempt to tackle exascale power and energy challenges, the majority of the implemented techniques have been designed to meet site-specific needs. There is no consensus among the stakeholders in academia, research and industry on which software components of modern HPC stack should be deployed and how they should interoperate. Coordination among these components is critical towards maximizing a target metric (such as FLOPS per watt) while meeting operating constraints (such as energy).

This realization led to the formation of the PowerStack Community in 2016 (https://www.osti.gov/biblio/1466153/). Its charter is to identify what power optimization software actors are needed, how they interoperate to streamline the optimization goals, and how to glue together existing open source production software for a cost-effective yet cohesive, cross-platform implementation of the software stack.

This poster solicits participation from members of academia, research, and industry, and invites the community to contribute towards this initiative of fine-tuning the current HPC stack to enable system-wide power optimization. The vision of this poster is to provide an overview of the PowerStack initiative, give a glimpse of some initial prototyping results, list multiple collaborators, point to relevant literature published within the community, and highlight various working groups that the reader can contribute to based on their background and expertise.

(PP05): Performance Conscious HPC (PeCoH) - 2019

Kai Himstedt (University of Hamburg)

In PeCoH, we establish the Hamburg HPC Competence Center (HHCC) as a virtual institution, which coordinates and fosters joint performance engineering activities between the local compute centers DKRZ, RRZ and TUHH RZ. Together, we will implement user services to support performance engineering on a basic level and provide a basis for co-development, user education and dissemination of performance engineering concepts. In this poster we focus on performance awareness, software engineering for HPC, and the development of our HPC certification program. Project outputs and ongoing activities are presented.

(PP06): The International HPC Certification Program

Julian Kunkel (University of Reading)

The HPC community has always considered the training of new and existing HPC practitioners to be of high importance to its growth. The significance of training will increase even further in the era of Exascale when HPC encompasses even more scientific disciplines. This diversification of HPC practitioners challenges the traditional training approaches, which are not able to satisfy the specific needs of users, often coming from non-traditionally HPC disciplines and only interested in learning a particular set of skills. HPC centres are struggling to identify and overcome the gaps in users' knowledge. How should we support prospective and existing users who are not aware of their own knowledge gaps? We started the establishment of the International HPC Certification program that aims to clearly categorize, define and examine HPC related skills. Oriented on the needs of practitioners, the program does not define a linear curriculum or interfere with content providers. Ultimately, we aim for the certificates to be recognized and respected by the HPC community and industry.

(PP07): ESiWACE : A European Centre of Excellence for Future Exascale Climate and Weather Predictions

Philipp Neumann (Deutsches Klimarechenzentrum (DKRZ))

The Centre of Excellence in Simulation of Weather and Climate in Europe (ESiWACE) forms a joint scientific community around Earth System Modelling (ESM) from the two communities of weather and climate research. The main objectives of ESiWACE are to substantially improve efficiency and productivity of numerical weather and climate simulation on high-performance computing (HPC) platforms, strengthening the user-driven evolution of the community software, build a critical mass and create expertise to increase the community impact on hardware development towards the extreme scale as well as future international exascale initiatives. Beside the three core themes and an introduction to the consecutive project ESiWACE2, the poster will focus on the central deliverable of global high resolution demonstrators.

(PP08): Rootless Containers with Udocker

Mário David (Laboratório de Instrumentação e Física Experimental de Partículas (LIP), Infraestrutura Nacional de Computação Distribuída (INCD))

udocker (https://github.com/indigo-dc/udocker) is a tool that addresses the problematic of executing Linux containers in user space, i.e. without installing additional system software, without requiring administrative privileges and in a way that respects resource usage policies, accounting and process controls. udocker empowers users to execute applications encapsulated in containers easily in any Linux system including computing clusters.

udocker implements a subset of Docker commands aimed at searching, pulling, importing, loading and executing containers. The self installation allows a user to transfer udocker and execute it to pull the required tools and libraries. All required binary tools and libraries are provided with udocker and compilation is not required. udocker is an integration tool that incorporates several execution methods giving the user the best possible options to run their containers according to the host capabilities. Several interchangeable execution modes are available, that exploit different technologies and tools, enabling udocker to run in older and newer Linux distributions. Currently udocker supports four modes: system call interception and pathname rewriting via PTRACE, dynamic library call interception and pathname rewriting via shared library preload, Linux unprivileged namespaces via runC, and also Singularity where available. Each approach has its own advantages and limitations, and therefore an integration tool offers flexibility and freedom of choice to adapt to the application and host characteristics.

udocker is been successfully used to support execution of HTC, HPC and GPGPU based applications in many datacenters and infrastructures, and has more than 500 stars on github.

(PP09): EPEEC: Productivity at Exascale

Antonio J. Peña (Barcelona Supercomputing Center (BSC))

EPEEC's main goal is to develop and deploy a production-ready parallel programming environment that turns upcoming overwhelmingly-heterogeneous exascale supercomputers into manageable platforms for domain application developers.

(PP10): EuroEXA - EU ExaScale Co-Design Project

Peter Hopton (Iceotope)

Funded by the EU, EuroEXA is a €20m co-design project as part of the EU race to ExaScale. EuroEXA inherits IP from other EU projects and has had donations of IP from major companies worth as much as €80m, making EuroEXA a €100m project.

EuroEXA's objective is to provide a template and demonstrator for an upcoming ExaScale system by co-designing and implementing a petascale-level prototype with ground-breaking characteristics. To accomplish this, the project takes a holistic approach innovating both across the technology and the application/system software pillars. EuroEXA proposes a balanced architecture for compute and data-intensive applications, that builds on top of cost-efficient, modular-integration enabled by novel inter-die links, utilises a novel processing unit and embraces FPGA acceleration for computational, networking and storage operations.

EuroEXA hardware designers work together with system software experts optimising the entire stack from language runtimes to low-level kernel drivers, and application developers that bring in a rich mix of key HPC applications from across climate/weather, physical/energy and life-science/bioinformatics domains to enable efficient system co-design and maximise the impact of the project.

EuroEXA has successfully deployed its first testbed at STFC Labs Daresbury and is working on the production of a second generation testbed with improvements to hardware and software technology as a result of the codesign process and strong innovation management.

(PP11): Middleware for Memory and Data-Awareness in Workflows (Maestro)
Manuel Arenaz (Appentra Solutions)

High Performance Computing (HPC) and High Performance Data Analytics (HPDA) opens up the opportunity to solve a wide variety of questions and challenges. The number and complexity of challenges that HPC and HPDA can help with are limited by the performance of computer software and hardware. Increasingly, performance is now limited by how fast data can be moved within the memory and storage of the hardware. So far, little work has been done to improve data movement.

How will Maestro help? Maestro will develop a new framework to improve the performance of data movement in HPC and HPDA, helping to improve the performance of software, and therefore the energy consumption and CPU hours used by software; and to encourage the uptake of HPC by new communities by lowering the memory performance barrier.

Maestro will consider two key components:

- Data movement awareness: Moving data in computer memory had not always been a performance bottleneck. Great improvements have been made in computational performance, but the software for memory has not changed during this time. Maestro will develop a better understanding of the performance barriers of data movement.

- Memory awareness: As memory becomes more complex, software performance is limited by data

movement across the layers of memory. To improve software performance it is now important that software has an 'awareness' of memory and how to optimise data movement.

Maestro has the potential to influence a broad range of human discovery and knowledge, as every computational application relies on data movement.

(PP12): ICEI: HPC Centres Delivering Federated E-Infrastructure Services
Anne Carstensen (Forschungszentrum Juelich)

The ICEI (Interactive Computing e-infrastructure for the Human Brain Project) project is funded by the European Commission under the Framework Partnership Agreement of the Human Brain Project (HBP). Five leading European Supercomputing Centres are working together to develop a set of e-infrastructure services that will be federated to form the Fenix Infrastructure. The centres (BSC, CEA, CINECA, ETHZ-CSCS and JUELICH-JSC) committed to perform a coordinated procurement of equipment, licences for software components and R&D services to realize elements of the e-infrastructure. Fenix Infrastructure services include elastic access to scalable and interactive compute resources and a federated data infrastructure. The distinguishing characteristic of this e-infrastructure is that data repositories and scalable supercomputing systems will be in close proximity and well integrated. User access is granted via a peer-review based allocation mechanism. The HBP is the initial prime and lead user community, guiding the infrastructure development in a use-case driven co-design approach. While the HBP is given a programmatic access to 25% of the resources, 15% are provided to European researchers at large via PRACE. The Fenix Infrastructure will deliver federated compute and data services to European researchers by aggregating capacity from multiple resource providers (Fenix MoU parties) and enabling access from existing community platforms, like for the HBP. In order to achieve these goals, the federation needs to rely on a robust and reliable authentication and authorisation infrastructure (AAI), a trustworthy environment where users can be managed and granted to access resources securely and as seamlessly, as possible.

(PP13): OCRE Cloud Benchmarking Validation Test Suite
Ignacio Peluaga (CERN, Universidad de Sevilla)

Helix Nebula Science Cloud (HNSciCloud) developed a hybrid cloud linking commercial cloud service providers and research organisations in-house resources via the GÉANT network. The hybrid platform offered data management capabilities with transparent data access, accessible via eduGAIN and ELIXIR AAI systems. The OCRE (Open Clouds for Research Environments) project will leverage the experience of HNSciCloud in the exploitation of commercial cloud services, currently being considered by the European research community as part of a hybrid cloud model to support the needs of their scientific programmes. To ensure that the cloud offerings conform to the tender requirements and satisfy the needs of the research community, OCRE is developing a cloud benchmarking validation test suite. The test-

suite leverages on the testing activities of HNSciCloud where a group of ten Research organisations (CERN, CNRS, DESY, EMBL-EBI, ESRF, INFN, IFAE, KIT, SURFsara and STFC) representing multiple use cases from several scientific domains, have put together more than thirty tests. These provide functional and performance benchmarks in several technical domains such as: compute, storage, HPC, GPUs, network connectivity performance, and advanced containerised cloud application deployments. The test-suite will be used to validate the technical readiness level of suppliers, in order to check whether these meet the community's requirements as stipulated in the OCRE tender specification. This tool is being designed to be as modular and autonomous as possible, using an abstraction layer based on Docker and Kubernetes for orchestration, using Terraform for resource provisioning, pushing the results to an S3 bucket at CERN.

(PP14): Advanced Computation and I/O Methods for Earth-System Simulations
Nabeeh Jum'ah (University of Hamburg)

The Advanced Computation and I/O Methods for Earth-System Simulations (AIMES) project addresses the key issues of programmability, computational efficiency and I/O limitations that are common in next-generation icosahedral earth-system models. Ultimately, the project is intended to foster development of best-practices and useful norms by cooperating on shared ideas and components. During the project, we will ensure that the developed concepts and tools are not only applicable for earth-science but for other scientific domains as well. In this poster we show the projects plan and progress and present some results.

(PP15): EXAHD -- Current Work on Scalable and Fault-Tolerant Plasma Simulations
Theresa Pollinger (Universität Stuttgart)

In this poster session, we give an overview on the SPPEXA project EXAHD. EXAHD focuses on the solution of a gyrokinetic system for plasma simulations. While the gyrokinetic formulation used in the GENE code is already reduced to five dimensions, a treatment of fully resolved tokamak geometries is still unfeasible due to the curse of dimensionality.

In EXAHD, we apply the Sparse Grid Combination Technique to decouple the problem into independent problems of lower resolution. By distributing them via a manager-worker pattern, we are able to scale GENE in our framework to up to 180225 cores. Even more, our approach allows for algorithmic fault tolerance: Missing solutions can be reconstructed from the neighboring solutions in case of silent errors and hardware failures without the need for expensive checkpoint-restart. Our results show that the Fault Tolerant Combination Technique allows for accurate results in the presence of hard and soft faults while maintaining high scalability.

The Combination Technique enables us to scale GENE even further -- we are therefore investigating the

pitfalls and possibilities of distributing the computation across HPC systems.

(PP16): The Movement Toward HPC Inclusivity: Achieving On-Demand Accessibility of High Performance Computing (HPC) in Ephemeral Projects
Cristin Merritt (Alces Flight Limited)

In June of 2016 the Alces Flight team, through our open-source work on the Gridware application delivery project, made the decision to explore on-demand public cloud consumption for High Performance Computing (HPC). We created Alces Flight Compute, a fully-featured, scalable HPC environment for research and scientific computing and provided it as a free subscription service to researchers in order to study how they would approach and consume this then new technology. Over the past three years we have worked with a range of HPC projects that employed differing levels of public-cloud adoption. The outcomes of each have demonstrated that regardless of the relative percentage of work completed on a public cloud, its usage has broadened the capabilities of researchers and enabled researchers to plan future activities with a broader scope with more inclusive design methodologies. Along the way we have gathered information on the strengths of public cloud for HPC, developed tools to help determine how public cloud could be suitable for current and future projects and workloads, and gathered insight into how investment into HPC solutions can operate when public cloud is an option for use. This project is now transitioning away from single-user, on-demand public cloud into open-source building blocks for HPC under the name OpenFlightHPC, launching in November, 2019.

(PP17): Secure Data Processing on Shared HPC Systems
Narges Zarrabi (SURFsara)

High performance computing (HPC) clusters operating in shared and batch mode pose challenges for processing sensitive data. Our platform as a service solution provides a customisable virtualized solution that addresses this without modifying existing HPC infrastructures. Using PCOCC and SLURM this platform can be used for processing sensitive data within a shared HPC environment and address both strict and flexible data security requirements.

(PP18): Harmony: A Harness Monitoring System for the Oak Ridge Leadership Computing Facility
Verónica G. Vergara Larrea (Oak Ridge National Laboratory)

Summit, the latest flagship supercomputer at the Oak Ridge Leadership Computing Facility (OLCF), and the number one system in the November 2018 Top500 list, completed its acceptance testing in 2018. Acceptance of a new system requires extensive testing and is comprised of hundreds of tests executed for several weeks. The acceptance test (AT) team utilizes the OLCF test harness to automate the launching and verification of these tests. Within this activity, analysis of test results is required to

understand and classify all test failures. The sheer number of tests involved makes performing these tasks challenging. To complete these tasks more efficiently, in addition to lessen the personnel burden during acceptance testing, we have developed a harness monitoring system for the OLCF test harness called Harmony.

Harmony consists of three distinct modules: monitoring, recording, and reporting modules. Harmony's monitoring module ensures that tests launched by the harness are progressing in the job queue and restarted correctly after any failure. It can send out alerts via multiple channels, including a custom Slack application and email to AT personnel regarding status of tests. The recording system ingests results generated by the test harness into a database, and automatically updates it with newly generated results. A Django-based website provides an interface for its reporting module to filter through tests, allowing us to analyze, describe, and categorize any test failure.

Harmony is open source and publicly available. This poster presents Harmony and shows how its modular design allows it to be customized for other useful purposes.

(PP19): Heterogeneous Computing for Deep Learning

Herman Lam (University of Florida, SHREC)

Mission-critical applications involving stringent constraints (latency, throughput, power, size, etc.) present computing challenges to achieve tradeoffs among these constraints, often resulting in inefficient or sub-optimal performance. Heterogeneous computing (CPU+GPU+FPGA) offers an opportunity to address this challenge and balance the tradeoffs for achieving application objectives. Our research team at the University of Florida is studying the application of heterogeneous computing to high-energy physics (HEP) with convolutional neural networks (CNNs). This poster presents early findings in adapting state-of-the-art CNN models for HEP data analysis on a heterogeneous platform, achieving an average of 2X speedup for inferencing with naive optimization. Our team won the first-ever DELL EMC AI Challenge.

(PP20): An Implementation of International Data Cloud

Weicheng Huang (National Center for High-Performance Computing, Taiwan)

Data needs to be shared and integrated to create values. The global data sharing between international partners requires a sustainable trust-based platform. In 2018, an international data cloud effort between AIST Japan and NCHC Taiwan has been initiated to prototype a platform for sharing both the data and the computing power.

Since the Data Cloud has the nature of distributed data across organizational boundaries, it has to tackle with data sharing and safety, user management, etc.

There are 4 major tasks to be tackled with, they are 1). Connecting both data centers, 2). Secured data sharing and exchange, 3). Accessing data center from AIoT devices, 4). User authentication and authorization.

This 4-year project was set out to tackle the issues above and provide a prototype of data cloud service with AI facilities integrated. In addition, an AI application is identified to demonstrate the feasibility of such a data cloud implementation

(PP21): LOWAIN Project (LOW Arithmetic INtensity Specific Architectures)
Ludek Kucera (Czech Technical University, Charles University)

When running the HPCG benchmark, conceived as a representative of supercomputer simulations, most modern supercomputers aren't using more than 1.5-2.0% of their peak computing power.

Extrapolating, a future Summit-like (peak) exascale supercomputer would execute ~15 PFlop/s when running the HPCG. The principal reason of poor HPCG behavior is low flop/byte ratio (counting just bytes crossing the processor-memory boundary!).

SpMV product, the key HPCG component, does MPY+ADD only for each matrix element brought from the memory, i.e., double-precision flop/byte is <=0.25, single-precision flop/byte <=0.5.

E.g., NVIDIA Volta-100 has memory bandwidth 900 GB/s, enough for <=225 SpMV DP GFlop/s, its DP peak computing power 7800 GFlop/s used for <=2.88%.

The first phase of LOWAIN aims to confirm that a wide class of simulations, e.g., NWP, CFD, mechanical deformation, combustion/explosion, exhibits the flop/byte ratio not much higher than the one of the HPCG (already done for the WRF program).

Since it is unlikely the memory bandwidth will be substantially increased in the near future (the Volta-100 memory bus has extremely high width 4096!), the first LOWAIN phase would justify development of application-specific computer architectures more efficient for low flop/byte problems, in particular a highly heretic idea of "exascale-equivalent" computers with the same low-F/B performance as a Summit-like exascale computer, but having strongly sub-exascale peak performance.

The second phase would be directed to design of intelligent memory systems to guarantee the best use of the limited memory bandwidth, since the cache-miss behavior and rather rigid pre-fetch tools of the existing systems are not sufficient.

(PP22): OpenFPM for Scalable Particle-Mesh Codes on CPUs and GPUs

Pietro Incardona (TU Dresden, Center for Systems Biology Dresden)

Scalable and efficient numerical simulations are of increasing importance in all areas of science and technology. This is fueled by a steady growth in the performance of computing hardware and increasing heterogeneous parallelism. However, efficiently implementing scalable simulation codes on heterogeneous, distributed hardware systems is the current bottleneck. This bottleneck can be relaxed by intermediate software layers that provide abstractions closer to the problem domain, allowing the computational scientist to focus on the simulation algorithm. Here, we present OpenFPM, an open and scalable framework that provides an abstraction layer for numerical simulations using particles and/or meshes. OpenFPM provides transparent and scalable infrastructure for shared-memory and distributed-memory implementations of hybrid particle-mesh simulations of both discrete and continuous models. This infrastructure is complemented with portable implementations of frequently used numerical routines, as well as interfaces to third-party libraries. We present the architecture and design of OpenFPM, detail the underlying abstractions, and benchmark the framework in applications ranging from Smoothed Particle Hydrodynamics (SPH) to Molecular Dynamics (MD), Discrete Element Methods (DEM), and stencil solvers, comparing it to the current state of the art and existing simulation software frameworks.

(PP23): MLS: Multilevel Scheduling in Large Scale High Performance Computers

Ahmed Eleliemy (University of Basel)

High performance computing systems are of increased size (in terms of node count, core count, and core types per node), resulting in increased available hardware parallelism. Hardware parallelism can be found at several levels, from machine instructions to global computing sites. Unfortunately, exposing, expressing, and exploiting parallelism is difficult when considering the increase in parallelism within each level and when exploiting more than a single or even a couple of parallelism levels.

The multilevel scheduling (MLS) project aims to offer an answer to the following research question: Given massive parallelism, at multiple levels, and of diverse forms and granularities, how can it be exposed, expressed, and exploited such that execution times are reduced, performance targets are achieved, and acceptable efficiency is maintained?

The MLS project investigates the development of a multilevel approach for achieving scalable scheduling in large scale high performance computing systems across the multiple levels of parallelism, with a focus on software parallelism. By integrating multiple levels of parallelism, MLS differs from hierarchical scheduling, traditionally employed to achieve scalability within a single level of parallelism. Specifically, MLS extends and bridges the most successful (batch, application, and thread) scheduling models beyond a single or a couple of parallelism levels (scaling across) and beyond their current scale (scaling out).

Via the MLS approach, the project aims to leverage all available parallelism and address hardware heterogeneity in large scale high performance computers such that execution times are reduced,

performance targets are achieved, and acceptable efficiency is maintained.

(PP24): Helping You Improve Software Sustainability and Development Productivity: An Overview of the IDEAS Project

David E. Bernholdt (Oak Ridge National Laboratory)

The IDEAS Productivity project (https://ideas-productivity.org) was established to help address challenges to software productivity and sustainability driven by the confluence of demands for predictive multiscale and multiphysics simulations, analysis, and design in computational science and engineering (CSE) and rapid and significant changes in the architectures of high-end computing systems (HPC).

IDEAS focuses on improving scientific productivity by qualitatively improving developer productivity (positively impacting product quality, development time, and staffing resources) and software sustainability (reducing the cost of maintaining, sustaining, and evolving software capabilities in the future)—thereby enabling a fundamentally different attitude to creating and supporting CSE applications.

We are working within the broader CSE/HPC community to help create an extreme-scale scientific software development ecosystem composed of high-quality, reusable CSE software components and libraries; a collection of best practices, processes, and tools; and substantial outreach mechanisms for promoting and disseminating productivity improvements. We intend to improve CSE productivity by enabling better, faster and cheaper CSE application capabilities for extreme-scale computing.

This poster will provide an overview of the IDEAS project's approach and activities, how you can benefit from this work, and how you can contribute to its further advancement.

(PP25): Holistic Approach to Energy Efficient HPC

Vadim Elisseev (IBM Research)

Upcoming High Performance Computing (HPC) systems are on the critical path towards delivering the highest level of performance for large scale applications. As supercomputers become larger in the drive to the next levels of performance, energy efficiency has emerged as one of the foremost design goals. New approaches for energy optimization are being explored which optimize throughout the whole HPC stack - from firmware and hardware through to the OS, application run-times and workload managers. The challenge of optimizing for energy efficiency requires an orchestrated approach across different components of the infrastructure. We present our approach to energy and power management, which can be described as Energy Aware Scheduling (EAS). EAS uses performance and power consumption models and software hardware co-design for implementing various energy/power aware scheduling policies at the node, job and cluster levels.

(PP26): Quantum Natural Language Processing

Venkatesh Kannan (Irish Centre for High-End Computing (ICHEC), National University of Ireland Galway (NUIG))

Natural language processing (NLP) is often used to perform tasks like sentiment analysis, relationship extraction and word sense disambiguation. Most traditional NLP algorithms operate over strings of words and are limited since they analyse meanings of the component words in a corpus without information about grammatical rules of the language. Consequently, the qualities of results of these traditional algorithms are often unsatisfactory with increase in problem complexity.

An alternate approach called “compositional semantics” incorporates the grammatical structure of sentences in a language into the analysis algorithms. One such model is “distributional compositional semantics” (DisCo) which gives grammatically informed algorithms that compute the meaning of sentences. This algorithm has been noted to offer significant improvements to the quality of results. However, the main challenge in its implementation is the need for large classical computational resources.

The DisCo model was developed by its authors with direct inspiration from quantum theory, and presents two quantum algorithms: the “closest vector problem” algorithm and the “CSC sentence similarity” algorithm. Their quantum implementation lowers storage and compute requirements compared to a classic HPC implementation.

In this project, the Irish Centre for High-End Computing collaborates with Intel Corporation to implement the two DisCo model quantum algorithms on the Intel Quantum Simulator deployed on the Irish national supercomputer. We target corpuses with ~2000 most common words using up to 41 qubits simulation. The implemented solution will be able to compute the meanings of two sentences (built from words in the corpus) and decide if their meanings match.

(PP27): SPH-EXA: Optimizing Smoothed Particle Hydrodynamics for Exascale Computing

Florina M. Ciorba (Universität Basel)

The SPH-EXA project, funded by the Swiss Platform for Advanced Scientific Computing, brings together expertise in High Performance Computing, Astrophysics, and Computational Fluid Dynamics. The Smoothed Particle Hydrodynamics (SPH) technique is a purely Lagrangian method, used in numerical simulations of fluids in astrophysics and computational fluid dynamics, among many other fields. SPH simulations are among the most computationally-demanding calculations, in terms of sustained floating-point operations per second, or FLOP/s. It is expected that these numerical simulations will significantly benefit from the future Exascale computing infrastructures, that will perform 1018 FLOP/s. The performance of the SPH codes is, in general, adversely impacted by several factors, such as multiple

time-stepping, long-range interactions, and/or boundary conditions. SPHYNX, ChaNGa, and SPH-flow, three SPH implementations, are the starting point of an interdisciplinary co-design project, SPH-EXA, for the development of an Exascale-ready SPH mini-app. The goal is to understand the scalability limitations of state-of-the-art SPH implementations and use such knowledge to create an Exascale-ready SPH mini-app. An extensive study of SPHYNX, ChaNGa, and SPH-flow has been performed, to gain insights and to expose the characteristics and any limitations of the codes. Such exposed limitations have been solved in the parent codes and shape the design and implementation of the SPH-EXA mini-app towards the use of efficient parallelization methods, fault-tolerance mechanisms, and load balancing approaches, to sustain the scalable execution of massively parallel SPH codes. The SPH-EXA mini-app development targets reproducibility and portability by using continuous integration systems, and containerization techniques.

(PP28): Evolutionary Convolutional Neural Network for High Energy Physics Detector Simulation
Sofia Vallecorsa (CERN)

High Energy Physics relies on Monte Carlo (MC) for different aspects of data analysis. MC simulation implement complex computations that, today, result in ~50% of CERN Computing Grid resources. Several alternative approaches are being investigated trading some accuracy for speed. Deep Learning approaches, for example, can result in x3000 speed-up while retaining 10% accuracy with respect to MC.

Design and optimisation of neural networks is very difficult and time consuming. Evolutionary computing could be exploited to improve this process, while providing the benefit of both network training and topology optimization in one step. By coding a neural network into genes and chromosome, Genetic Algorithms (GA) would exhibit numerous advantages: easily parallelizable, they could help reach global instead of local optima often selected by Stochastic Gradient Descent (SGD); they could also be combined to SGD for fine tuning.

Our project intends to use GA to train and optimise a 3-dimensional Convolutional Generative Adversarial Network we have developed for particle detector simulation. It is implemented in a few steps: a first phase, will implement a simplified version of our GAN network, focusing on one of the two networks that constitute the GAN (the “discriminator”). We will design a first prototype and define the method applicability (in terms of network complexity and computing resources). We will gradually increase the complexity of the problem, in terms of input image size and network features and finally implement the full adversarial training approach. We will compare performances to standard SGD and classical optimisation approaches (i.e. Bayesian).

(PP29): Cygnus: A Multi-Hybrid Supercomputing Platform with GPUs and FPGAs
Taisuke Boku (University of Tsukuba)

Graphics processing units (GPUs) have been widely used in high-performance computing (HPC) systems as accelerators because they can offer good peak performance and high memory bandwidth. However, the GPU is not almighty as an accelerator because it is not effective in applications that employ complicated algorithms using exception, non single-instruction-multiple-data streams (SIMD), partially poor parallelism, etc. To address these problems, field programmable gate arrays (FPGAs) have gained attention in HPC research because their computation and communication capabilities have dramatically improved in recent years as a result of improvements to semiconductor integration technologies that depend on Moore's Law. In addition to FPGA performance improvements, OpenCL-based FPGA development toolchains have been developed and offered by FPGA vendors, which reduces the programming effort required as compared to the past, and as a result, the interest in the FPGA from HPC field has been more increased. In this project, we make FPGAs cooperate with GPUs and utilize both accelerators complementarily in order to maximize the FPGA potential and to apply it to GPU-based HPC systems. We propose how to use FPGA for HPC which enables on-the-fly offloading computation at which CPUs/GPUs perform poorly to FPGAs while performing low-latency intra/inter-node communication, build a programming framework to comprehensively control these functionalities from the CPU, and demonstrate the effectiveness of our proposed approach by applying it to computational science applications.

(PP30): Deep Learning for Satellite Imagery

Sofia Vallecorsa (CERN)

Our project is a unique partnership between CERN, Intel, and the United Nations Institute for Training and Research (UNITAR) to use Deep Learning (DL) to improve the analysis of optical satellite imagery for humanitarian purposes. The core objective is to create spectrally valid simulated high-resolution satellite imagery depicting humanitarian situations such as refugee settlements, flood conditions, damaged infrastructure, and more, by using techniques such as Generative Adversarial Networks (GANs). UNITAR hosts the UN Operational Satellite Applications Centre (UNOSAT), which uses satellite imagery to support disaster response, humanitarian operations, and other activities of the broader UN system. UNITAR has in recent years started studying the application of DL to satellite imagery analysis, in order to improve efficiency in the many manual tasks frequently required: for example, digitizing a refugee settlement in a satellite image can take many hours, sometimes days of effort. Mapping displaced persons across broad regions such as northwest Syria can in turn be weeks of work. DL methods could greatly reduce the amount of time needed to complete such tasks: a key factor to an effective deployment of field operations in critical humanitarian situations. High-resolution satellite imagery is often licensed in such a way that it can be difficult to share it across UNITAR, UN partners, and academic organizations, reducing the amount of data available to train DL models. This fact has inhibited UNITARs DL research possibilities in various ways. The creation of realistic and spectrally accurate simulated images could enable and stimulate data sharing.

Wednesday, June 19th

Room: Booth N-230
10:00 am - 6:00 pm

Project Poster

Room: Booth N-230
3:15 pm - 4:00 pm

Project Poster Presentation

(PP01): TaLPas: Task-Based Load Balancing and Auto-Tuning in Particle Simulations
Philipp Neumann (University Hamburg - Department of Informatics)

TaLPas will provide a solution to fast and robust simulation of many, inter-dependent particle systems in peta- and exascale supercomputing environments. This will be beneficial for a wide range of applications, including sampling in molecular dynamics (rare event sampling, determination of equations of state, etc.), uncertainty quantification (sensitivity investigation of parameters on actual simulation results), or parameter identification (identification of optimal parameter sets to fit numerical model and experiment).

For this purpose, TaLPas targets 1. the development of innovative auto-tuning based particle simulation software in form of an open-source library to leverage optimal node-level performance. This will guarantee an optimal time-to-solution for small- to mid-sized particle simulations, 2. the development of a scalable workflow manager to optimally distribute inter-dependent particle simulation tasks on available HPC compute resources, 3. the investigation of performance prediction methods for particle simulations to support auto-tuning and to feed the workflow manager with accurate runtime predictions, 4. the integration of auto-tuning based particle simulation, scalable workflow manager and performance prediction, augmented by visualization of the sampling (parameter space exploration) and an approach to resilience. The latter will guarantee robustness at peta- and exascale.

Work presented at ISC will focus on steps 1-3. The integration of all components (step 4) is anticipated for the year 2019. To reach its goals, TaLPas bundles interdisciplinary expert knowledge on high-performance computing, visualization and resilience, performance modeling, and particle applications.

(PP02): The Virtual Institute for I/O and the IO-500
Julian Kunkel (University of Reading)

The research community in high-performance computing is organized loosely. There are many distinct resources such as homepages of research groups and benchmarks. The Virtual Institute for I/O aims to provide a hub for the community and particularly newcomers to find relevant information in many directions. It hosts the comprehensive data center list (CDCL). Similarly to the top500, it contains information about supercomputers and their storage systems.

I/O benchmarking, particularly, the intercomparison of measured performance between sites is tricky as there are more hardware components involved and configurations to take into account. Therefore, together with the community, we standardized an HPC I/O benchmark, the IO-500benchmark, for which the first list had been released during supercomputing in Nov. 2017. Such a benchmark is also useful to assess the impact of system issues like the Meltdown and Spectre* bugs.

This poster introduces the Virtual Institute for I/O, the high-performance storage list and the effort for the IO-500 which are unfunded community projects.

(PP03): NeIC presents Nordic Project Highlights: Nordic Resource Exchange & Highly-Available Storage Within Nordic LHC Tier-1

Michaela Barth (NeIC, NordForsk; PDC-HPC, KTH Royal Institute of Technology)

Through the Nordic e-Infrastructure Collaboration (NeIC) together the Nordic countries are tackling e-infrastructure challenges beyond singular national capabilities. Specific aspects of two current NeIC projects are highlighted on this poster.

Dellingr, NeIC's cross-border resource sharing project, contributes towards establishing a framework for resource sharing across the Nordics. Based on the experience of the first pilot the intented improved resource access process is presented. Allocations will use billing units (BU) as a common currency and the Waldur cloud brokerage framework (https://share.neic.no) will be the central tool used throughout the whole process starting from resource application, over usage tracking to linking to resulting publications. https://dellingr.neic.no/apply/

Within the context of the Nordic Large Hadron Collider (LHC) Computing Tier-1 the effective high-availability routines since 2016 are presented. Conceived in 2002 as a one-of-a-kind facility unifying six academic computing centres in four different countries, the Nordic Tier-1 can now look back on more than 13 years of successful operations with an excellent track record on reliability and availability. Using the High-Availability (HA) features within dCache, ucarpd for automatic IP fail-over, HAProxy for load balancing and Ganeti as well as repmgr for managing VMs and HA PostgreSQL, no downtimes have to be scheduled for regular Linux security updates or dCache upgrades and no restrictions for the perceived user experience apply.

(PP04): The HPC PowerStack: A Community-Driven Collaboration Towards an Energy Efficient Software Stack

Siddhartha Jana (Energy Efficient HPC Working Group, Intel Corporation)

While there exist several standalone efforts that attempt to tackle exascale power and energy challenges, the majority of the implemented techniques have been designed to meet site-specific needs. There is no consensus among the stakeholders in academia, research and industry on which software components of modern HPC stack should be deployed and how they should interoperate. Coordination among these components is critical towards maximizing a target metric (such as FLOPS per watt) while meeting operating constraints (such as energy).

This realization led to the formation of the PowerStack Community in 2016 (https://www.osti.gov/biblio/1466153/). Its charter is to identify what power optimization software actors are needed, how they interoperate to streamline the optimization goals, and how to glue together existing open source production software for a cost-effective yet cohesive, cross-platform implementation of the software stack.

This poster solicits participation from members of academia, research, and industry, and invites the community to contribute towards this initiative of fine-tuning the current HPC stack to enable system-wide power optimization. The vision of this poster is to provide an overview of the PowerStack initiative, give a glimpse of some initial prototyping results, list multiple collaborators, point to relevant literature published within the community, and highlight various working groups that the reader can contribute to based on their background and expertise.

(PP05): Performance Conscious HPC (PeCoH) - 2019

Kai Himstedt (University of Hamburg)

In PeCoH, we establish the Hamburg HPC Competence Center (HHCC) as a virtual institution, which coordinates and fosters joint performance engineering activities between the local compute centers DKRZ, RRZ and TUHH RZ. Together, we will implement user services to support performance engineering on a basic level and provide a basis for co-development, user education and dissemination of performance engineering concepts. In this poster we focus on performance awareness, software engineering for HPC, and the development of our HPC certification program. Project outputs and ongoing activities are presented.

(PP06): The International HPC Certification Program

Julian Kunkel (University of Reading)

The HPC community has always considered the training of new and existing HPC practitioners to be of high importance to its growth. The significance of training will increase even further in the era of Exascale when HPC encompasses even more scientific disciplines. This diversification of HPC practitioners challenges the traditional training approaches, which are not able to satisfy the specific needs of users, often coming from non-traditionally HPC disciplines and only interested in learning a particular set of skills. HPC centres are struggling to identify and overcome the gaps in users' knowledge. How should we support prospective and existing users who are not aware of their own knowledge gaps? We started the establishment of the International HPC Certification program that aims to clearly categorize, define and examine HPC related skills. Oriented on the needs of practitioners, the program does not define a linear curriculum or interfere with content providers. Ultimately, we aim for the certificates to be recognized and respected by the HPC community and industry.

(PP07): ESiWACE : A European Centre of Excellence for Future Exascale Climate and Weather Predictions

Philipp Neumann (Deutsches Klimarechenzentrum (DKRZ))

The Centre of Excellence in Simulation of Weather and Climate in Europe (ESiWACE) forms a joint scientific community around Earth System Modelling (ESM) from the two communities of weather and climate research. The main objectives of ESiWACE are to substantially improve efficiency and productivity of numerical weather and climate simulation on high-performance computing (HPC) platforms, strengthening the user-driven evolution of the community software, build a critical mass and create expertise to increase the community impact on hardware development towards the extreme scale as well as future international exascale initiatives. Beside the three core themes and an introduction to the consecutive project ESiWACE2, the poster will focus on the central deliverable of global high resolution demonstrators.

(PP08): Rootless Containers with Udocker

Mário David (Laboratório de Instrumentação e Física Experimental de Partículas (LIP), Infraestrutura Nacional de Computação Distribuída (INCD))

udocker (https://github.com/indigo-dc/udocker) is a tool that addresses the problematic of executing Linux containers in user space, i.e. without installing additional system software, without requiring administrative privileges and in a way that respects resource usage policies, accounting and process controls. udocker empowers users to execute applications encapsulated in containers easily in any Linux system including computing clusters.

udocker implements a subset of Docker commands aimed at searching, pulling, importing, loading and executing containers. The self installation allows a user to transfer udocker and execute it to pull the required tools and libraries. All required binary tools and libraries are provided with udocker and

compilation is not required. udocker is an integration tool that incorporates several execution methods giving the user the best possible options to run their containers according to the host capabilities. Several interchangeable execution modes are available, that exploit different technologies and tools, enabling udocker to run in older and newer Linux distributions. Currently udocker supports four modes: system call interception and pathname rewriting via PTRACE, dynamic library call interception and pathname rewriting via shared library preload, Linux unprivileged namespaces via runC, and also Singularity where available. Each approach has its own advantages and limitations, and therefore an integration tool offers flexibility and freedom of choice to adapt to the application and host characteristics.

udocker is been successfully used to support execution of HTC, HPC and GPGPU based applications in many datacenters and infrastructures, and has more than 500 stars on github.

(PP09): EPEEC: Productivity at Exascale

Antonio J. Peña (Barcelona Supercomputing Center (BSC))

EPEEC's main goal is to develop and deploy a production-ready parallel programming environment that turns upcoming overwhelmingly-heterogeneous exascale supercomputers into manageable platforms for domain application developers.

(PP10): EuroEXA - EU ExaScale Co-Design Project

Peter Hopton (Iceotope)

Funded by the EU, EuroEXA is a €20m co-design project as part of the EU race to ExaScale. EuroEXA inherits IP from other EU projects and has had donations of IP from major companies worth as much as €80m, making EuroEXA a €100m project.

EuroEXA's objective is to provide a template and demonstrator for an upcoming ExaScale system by co-designing and implementing a petascale-level prototype with ground-breaking characteristics. To accomplish this, the project takes a holistic approach innovating both across the technology and the application/system software pillars. EuroEXA proposes a balanced architecture for compute and data-intensive applications, that builds on top of cost-efficient, modular-integration enabled by novel inter-die links, utilises a novel processing unit and embraces FPGA acceleration for computational, networking and storage operations.

EuroEXA hardware designers work together with system software experts optimising the entire stack from language runtimes to low-level kernel drivers, and application developers that bring in a rich mix of key HPC applications from across climate/weather, physical/energy and life-science/bioinformatics domains to enable efficient system co-design and maximise the impact of the project.

EuroEXA has successfully deployed its first testbed at STFC Labs Daresbury and is working on the production of a second generation testbed with improvements to hardware and software technology as a result of the codesign process and strong innovation management.

(PP11): Middleware for Memory and Data-Awareness in Workflows (Maestro)
Manuel Arenaz (Appentra Solutions)

High Performance Computing (HPC) and High Performance Data Analytics (HPDA) opens up the opportunity to solve a wide variety of questions and challenges. The number and complexity of challenges that HPC and HPDA can help with are limited by the performance of computer software and hardware. Increasingly, performance is now limited by how fast data can be moved within the memory and storage of the hardware. So far, little work has been done to improve data movement.

How will Maestro help? Maestro will develop a new framework to improve the performance of data movement in HPC and HPDA, helping to improve the performance of software, and therefore the energy consumption and CPU hours used by software; and to encourage the uptake of HPC by new communities by lowering the memory performance barrier.

Maestro will consider two key components:

- Data movement awareness: Moving data in computer memory had not always been a performance bottleneck. Great improvements have been made in computational performance, but the software for memory has not changed during this time. Maestro will develop a better understanding of the performance barriers of data movement.

- Memory awareness: As memory becomes more complex, software performance is limited by data movement across the layers of memory. To improve software performance it is now important that software has an 'awareness' of memory and how to optimise data movement.

Maestro has the potential to influence a broad range of human discovery and knowledge, as every computational application relies on data movement.

(PP12): ICEI: HPC Centres Delivering Federated E-Infrastructure Services
Anne Carstensen (Forschungszentrum Juelich)

The ICEI (Interactive Computing e-infrastructure for the Human Brain Project) project is funded by the European Commission under the Framework Partnership Agreement of the Human Brain Project (HBP). Five leading European Supercomputing Centres are working together to develop a set of e-infrastructure services that will be federated to form the Fenix Infrastructure. The centres (BSC, CEA, CINECA, ETHZ-

CSCS and JUELICH-JSC) committed to perform a coordinated procurement of equipment, licences for software components and R&D services to realize elements of the e-infrastructure. Fenix Infrastructure services include elastic access to scalable and interactive compute resources and a federated data infrastructure. The distinguishing characteristic of this e-infrastructure is that data repositories and scalable supercomputing systems will be in close proximity and well integrated. User access is granted via a peer-review based allocation mechanism. The HBP is the initial prime and lead user community, guiding the infrastructure development in a use-case driven co-design approach. While the HBP is given a programmatic access to 25% of the resources, 15% are provided to European researchers at large via PRACE. The Fenix Infrastructure will deliver federated compute and data services to European researchers by aggregating capacity from multiple resource providers (Fenix MoU parties) and enabling access from existing community platforms, like for the HBP. In order to achieve these goals, the federation needs to rely on a robust and reliable authentication and authorisation infrastructure (AAI), a trustworthy environment where users can be managed and granted to access resources securely and as seamlessly, as possible.

(PP13): OCRE Cloud Benchmarking Validation Test Suite

Ignacio Peluaga (CERN, Universidad de Sevilla)

Helix Nebula Science Cloud (HNSciCloud) developed a hybrid cloud linking commercial cloud service providers and research organisations in-house resources via the GÉANT network. The hybrid platform offered data management capabilities with transparent data access, accessible via eduGAIN and ELIXIR AAI systems. The OCRE (Open Clouds for Research Environments) project will leverage the experience of HNSciCloud in the exploitation of commercial cloud services, currently being considered by the European research community as part of a hybrid cloud model to support the needs of their scientific programmes. To ensure that the cloud offerings conform to the tender requirements and satisfy the needs of the research community, OCRE is developing a cloud benchmarking validation test suite. The test-suite leverages on the testing activities of HNSciCloud where a group of ten Research organisations (CERN, CNRS, DESY, EMBL-EBI, ESRF, INFN, IFAE, KIT, SURFsara and STFC) representing multiple use cases from several scientific domains, have put together more than thirty tests. These provide functional and performance benchmarks in several technical domains such as: compute, storage, HPC, GPUs, network connectivity performance, and advanced containerised cloud application deployments. The test-suite will be used to validate the technical readiness level of suppliers, in order to check whether these meet the community's requirements as stipulated in the OCRE tender specification. This tool is being designed to be as modular and autonomous as possible, using an abstraction layer based on Docker and Kubernetes for orchestration, using Terraform for resource provisioning, pushing the results to an S3 bucket at CERN.

(PP14): Advanced Computation and I/O Methods for Earth-System Simulations

Nabeeh Jum'ah (University of Hamburg)

The Advanced Computation and I/O Methods for Earth-System Simulations (AIMES) project addresses the key issues of programmability, computational efficiency and I/O limitations that are common in next-generation icosahedral earth-system models. Ultimately, the project is intended to foster development of best-practices and useful norms by cooperating on shared ideas and components. During the project, we will ensure that the developed concepts and tools are not only applicable for earth-science but for other scientific domains as well. In this poster we show the projects plan and progress and present some results.

(PP15): EXAHD -- Current Work on Scalable and Fault-Tolerant Plasma Simulations
Theresa Pollinger (Universität Stuttgart)

In this poster session, we give an overview on the SPPEXA project EXAHD. EXAHD focuses on the solution of a gyrokinetic system for plasma simulations. While the gyrokinetic formulation used in the GENE code is already reduced to five dimensions, a treatment of fully resolved tokamak geometries is still unfeasible due to the curse of dimensionality.

In EXAHD, we apply the Sparse Grid Combination Technique to decouple the problem into independent problems of lower resolution. By distributing them via a manager-worker pattern, we are able to scale GENE in our framework to up to 180225 cores. Even more, our approach allows for algorithmic fault tolerance: Missing solutions can be reconstructed from the neighboring solutions in case of silent errors and hardware failures without the need for expensive checkpoint-restart. Our results show that the Fault Tolerant Combination Technique allows for accurate results in the presence of hard and soft faults while maintaining high scalability.

The Combination Technique enables us to scale GENE even further -- we are therefore investigating the pitfalls and possibilities of distributing the computation across HPC systems.

(PP16): The Movement Toward HPC Inclusivity: Achieving On-Demand Accessibility of High Performance Computing (HPC) in Ephemeral Projects
Cristin Merritt (Alces Flight Limited)

In June of 2016 the Alces Flight team, through our open-source work on the Gridware application delivery project, made the decision to explore on-demand public cloud consumption for High Performance Computing (HPC). We created Alces Flight Compute, a fully-featured, scalable HPC environment for research and scientific computing and provided it as a free subscription service to researchers in order to study how they would approach and consume this then new technology. Over the past three years we have worked with a range of HPC projects that employed differing levels of public-cloud adoption. The outcomes of each have demonstrated that regardless of the relative percentage of work completed on a

public cloud, its usage has broadened the capabilities of researchers and enabled researchers to plan future activities with a broader scope with more inclusive design methodologies. Along the way we have gathered information on the strengths of public cloud for HPC, developed tools to help determine how public cloud could be suitable for current and future projects and workloads, and gathered insight into how investment into HPC solutions can operate when public cloud is an option for use. This project is now transitioning away from single-user, on-demand public cloud into open-source building blocks for HPC under the name OpenFlightHPC, launching in November, 2019.

(PP17): Secure Data Processing on Shared HPC Systems
Narges Zarrabi (SURFsara)

High performance computing (HPC) clusters operating in shared and batch mode pose challenges for processing sensitive data. Our platform as a service solution provides a customisable virtualized solution that addresses this without modifying existing HPC infrastructures. Using PCOCC and SLURM this platform can be used for processing sensitive data within a shared HPC environment and address both strict and flexible data security requirements.

(PP18): Harmony: A Harness Monitoring System for the Oak Ridge Leadership Computing Facility
Verónica G. Vergara Larrea (Oak Ridge National Laboratory)

Summit, the latest flagship supercomputer at the Oak Ridge Leadership Computing Facility (OLCF), and the number one system in the November 2018 Top500 list, completed its acceptance testing in 2018. Acceptance of a new system requires extensive testing and is comprised of hundreds of tests executed for several weeks. The acceptance test (AT) team utilizes the OLCF test harness to automate the launching and verification of these tests. Within this activity, analysis of test results is required to understand and classify all test failures. The sheer number of tests involved makes performing these tasks challenging. To complete these tasks more efficiently, in addition to lessen the personnel burden during acceptance testing, we have developed a harness monitoring system for the OLCF test harness called Harmony.

Harmony consists of three distinct modules: monitoring, recording, and reporting modules. Harmony's monitoring module ensures that tests launched by the harness are progressing in the job queue and restarted correctly after any failure. It can send out alerts via multiple channels, including a custom Slack application and email to AT personnel regarding status of tests. The recording system ingests results generated by the test harness into a database, and automatically updates it with newly generated results. A Django-based website provides an interface for its reporting module to filter through tests, allowing us to analyze, describe, and categorize any test failure.

Harmony is open source and publicly available. This poster presents Harmony and shows how its

modular design allows it to be customized for other useful purposes.

(PP19): Heterogeneous Computing for Deep Learning

Herman Lam (University of Florida, SHREC)

Mission-critical applications involving stringent constraints (latency, throughput, power, size, etc.) present computing challenges to achieve tradeoffs among these constraints, often resulting in inefficient or sub-optimal performance. Heterogeneous computing (CPU+GPU+FPGA) offers an opportunity to address this challenge and balance the tradeoffs for achieving application objectives. Our research team at the University of Florida is studying the application of heterogeneous computing to high-energy physics (HEP) with convolutional neural networks (CNNs). This poster presents early findings in adapting state-of-the-art CNN models for HEP data analysis on a heterogeneous platform, achieving an average of 2X speedup for inferencing with naive optimization. Our team won the first-ever DELL EMC AI Challenge.

(PP20): An Implementation of International Data Cloud

Weicheng Huang (National Center for High-Performance Computing, Taiwan)

Data needs to be shared and integrated to create values. The global data sharing between international partners requires a sustainable trust-based platform. In 2018, an international data cloud effort between AIST Japan and NCHC Taiwan has been initiated to prototype a platform for sharing both the data and the computing power.

Since the Data Cloud has the nature of distributed data across organizational boundaries, it has to tackle with data sharing and safety, user management, etc.

There are 4 major tasks to be tackled with, they are 1). Connecting both data centers, 2). Secured data sharing and exchange, 3). Accessing data center from AIoT devices, 4). User authentication and authorization.

This 4-year project was set out to tackle the issues above and provide a prototype of data cloud service with AI facilities integrated. In addition, an AI application is identified to demonstrate the feasibility of such a data cloud implementation

(PP21): LOWAIN Project (LOW Arithmetic INtensity Specific Architectures)

Ludek Kucera (Czech Technical University, Charles University)

When running the HPCG benchmark, conceived as a representative of supercomputer simulations, most modern supercomputers aren’t using more than 1.5-2.0% of their peak computing power.

Extrapolating, a future Summit-like (peak) exascale supercomputer would execute ~15 PFlop/s when running the HPCG. The principal reason of poor HPCG behavior is low flop/byte ratio (counting just bytes crossing the processor-memory boundary!).

SpMV product, the key HPCG component, does MPY+ADD only for each matrix element brought from the memory, i.e., double-precision flop/byte is <=0.25, single-precision flop/byte <=0.5.

E.g., NVIDIA Volta-100 has memory bandwidth 900 GB/s, enough for <=225 SpMV DP GFlop/s, its DP peak computing power 7800 GFlop/s used for <=2.88%.

The first phase of LOWAIN aims to confirm that a wide class of simulations, e.g., NWP, CFD, mechanical deformation, combustion/explosion, exhibits the flop/byte ratio not much higher than the one of the HPCG (already done for the WRF program).

Since it is unlikely the memory bandwidth will be substantially increased in the near future (the Volta-100 memory bus has extremely high width 4096!), the first LOWAIN phase would justify development of application-specific computer architectures more efficient for low flop/byte problems, in particular a highly heretic idea of “exascale-equivalent” computers with the same low-F/B performance as a Summit-like exascale computer, but having strongly sub-exascale peak performance.

The second phase would be directed to design of intelligent memory systems to guarantee the best use of the limited memory bandwidth, since the cache-miss behavior and rather rigid pre-fetch tools of the existing systems are not sufficient.

(PP22): OpenFPM for Scalable Particle-Mesh Codes on CPUs and GPUs

Pietro Incardona (TU Dresden, Center for Systems Biology Dresden)

Scalable and efficient numerical simulations are of increasing importance in all areas of science and technology. This is fueled by a steady growth in the performance of computing hardware and increasing heterogeneous parallelism. However, efficiently implementing scalable simulation codes on heterogeneous, distributed hardware systems is the current bottleneck. This bottleneck can be relaxed by intermediate software layers that provide abstractions closer to the problem domain, allowing the computational scientist to focus on the simulation algorithm. Here, we present OpenFPM, an open and scalable framework that provides an abstraction layer for numerical simulations using particles and/or meshes. OpenFPM provides transparent and scalable infrastructure for shared-memory and distributed-memory implementations of hybrid particle-mesh simulations of both discrete and continuous models. This infrastructure is complemented with portable implementations of frequently used numerical routines, as well as interfaces to third-party libraries. We present the architecture and design of OpenFPM, detail the underlying abstractions, and benchmark the framework in applications ranging from Smoothed

Particle Hydrodynamics (SPH) to Molecular Dynamics (MD), Discrete Element Methods (DEM), and stencil solvers, comparing it to the current state of the art and existing simulation software frameworks.

(PP23): MLS: Multilevel Scheduling in Large Scale High Performance Computers
Ahmed Eleliemy (University of Basel)

High performance computing systems are of increased size (in terms of node count, core count, and core types per node), resulting in increased available hardware parallelism. Hardware parallelism can be found at several levels, from machine instructions to global computing sites. Unfortunately, exposing, expressing, and exploiting parallelism is difficult when considering the increase in parallelism within each level and when exploiting more than a single or even a couple of parallelism levels.

The multilevel scheduling (MLS) project aims to offer an answer to the following research question: Given massive parallelism, at multiple levels, and of diverse forms and granularities, how can it be exposed, expressed, and exploited such that execution times are reduced, performance targets are achieved, and acceptable efficiency is maintained?

The MLS project investigates the development of a multilevel approach for achieving scalable scheduling in large scale high performance computing systems across the multiple levels of parallelism, with a focus on software parallelism. By integrating multiple levels of parallelism, MLS differs from hierarchical scheduling, traditionally employed to achieve scalability within a single level of parallelism. Specifically, MLS extends and bridges the most successful (batch, application, and thread) scheduling models beyond a single or a couple of parallelism levels (scaling across) and beyond their current scale (scaling out).

Via the MLS approach, the project aims to leverage all available parallelism and address hardware heterogeneity in large scale high performance computers such that execution times are reduced, performance targets are achieved, and acceptable efficiency is maintained.

(PP24): Helping You Improve Software Sustainability and Development Productivity: An Overview of the IDEAS Project
David E. Bernholdt (Oak Ridge National Laboratory)

The IDEAS Productivity project (https://ideas-productivity.org) was established to help address challenges to software productivity and sustainability driven by the confluence of demands for predictive multiscale and multiphysics simulations, analysis, and design in computational science and engineering (CSE) and rapid and significant changes in the architectures of high-end computing systems (HPC).

IDEAS focuses on improving scientific productivity by qualitatively improving developer productivity (positively impacting product quality, development time, and staffing resources) and software

sustainability (reducing the cost of maintaining, sustaining, and evolving software capabilities in the future)—thereby enabling a fundamentally different attitude to creating and supporting CSE applications.

We are working within the broader CSE/HPC community to help create an extreme-scale scientific software development ecosystem composed of high-quality, reusable CSE software components and libraries; a collection of best practices, processes, and tools; and substantial outreach mechanisms for promoting and disseminating productivity improvements. We intend to improve CSE productivity by enabling better, faster and cheaper CSE application capabilities for extreme-scale computing.

This poster will provide an overview of the IDEAS project's approach and activities, how you can benefit from this work, and how you can contribute to its further advancement.

(PP25): Holistic Approach to Energy Efficient HPC

Vadim Elisseev (IBM Research)

Upcoming High Performance Computing (HPC) systems are on the critical path towards delivering the highest level of performance for large scale applications. As supercomputers become larger in the drive to the next levels of performance, energy efficiency has emerged as one of the foremost design goals. New approaches for energy optimization are being explored which optimize throughout the whole HPC stack - from firmware and hardware through to the OS, application run-times and workload managers. The challenge of optimizing for energy efficiency requires an orchestrated approach across different components of the infrastructure. We present our approach to energy and power management, which can be described as Energy Aware Scheduling (EAS). EAS uses performance and power consumption models and software hardware co-design for implementing various energy/power aware scheduling policies at the node, job and cluster levels.

(PP26): Quantum Natural Language Processing

Venkatesh Kannan (Irish Centre for High-End Computing (ICHEC), National University of Ireland Galway (NUIG))

Natural language processing (NLP) is often used to perform tasks like sentiment analysis, relationship extraction and word sense disambiguation. Most traditional NLP algorithms operate over strings of words and are limited since they analyse meanings of the component words in a corpus without information about grammatical rules of the language. Consequently, the qualities of results of these traditional algorithms are often unsatisfactory with increase in problem complexity.

An alternate approach called "compositional semantics" incorporates the grammatical structure of sentences in a language into the analysis algorithms. One such model is "distributional compositional semantics" (DisCo) which gives grammatically informed algorithms that compute the meaning of

sentences. This algorithm has been noted to offer significant improvements to the quality of results. However, the main challenge in its implementation is the need for large classical computational resources.

The DisCo model was developed by its authors with direct inspiration from quantum theory, and presents two quantum algorithms: the “closest vector problem” algorithm and the “CSC sentence similarity” algorithm. Their quantum implementation lowers storage and compute requirements compared to a classic HPC implementation.

In this project, the Irish Centre for High-End Computing collaborates with Intel Corporation to implement the two DisCo model quantum algorithms on the Intel Quantum Simulator deployed on the Irish national supercomputer. We target corpuses with ~2000 most common words using up to 41 qubits simulation. The implemented solution will be able to compute the meanings of two sentences (built from words in the corpus) and decide if their meanings match.

(PP27): SPH-EXA: Optimizing Smoothed Particle Hydrodynamics for Exascale Computing
Florina M. Ciorba (Universität Basel)

The SPH-EXA project, funded by the Swiss Platform for Advanced Scientific Computing, brings together expertise in High Performance Computing, Astrophysics, and Computational Fluid Dynamics. The Smoothed Particle Hydrodynamics (SPH) technique is a purely Lagrangian method, used in numerical simulations of fluids in astrophysics and computational fluid dynamics, among many other fields. SPH simulations are among the most computationally-demanding calculations, in terms of sustained floating-point operations per second, or FLOP/s. It is expected that these numerical simulations will significantly benefit from the future Exascale computing infrastructures, that will perform 1018 FLOP/s. The performance of the SPH codes is, in general, adversely impacted by several factors, such as multiple time-stepping, long-range interactions, and/or boundary conditions. SPHYNX, ChaNGa, and SPH-flow, three SPH implementations, are the starting point of an interdisciplinary co-design project, SPH-EXA, for the development of an Exascale-ready SPH mini-app. The goal is to understand the scalability limitations of state-of-the-art SPH implementations and use such knowledge to create an Exascale-ready SPH mini-app. An extensive study of SPHYNX, ChaNGa, and SPH-flow has been performed, to gain insights and to expose the characteristics and any limitations of the codes. Such exposed limitations have been solved in the parent codes and shape the design and implementation of the SPH-EXA mini-app towards the use of efficient parallelization methods, fault-tolerance mechanisms, and load balancing approaches, to sustain the scalable execution of massively parallel SPH codes. The SPH-EXA mini-app development targets reproducibility and portability by using continuous integration systems, and containerization techniques.

(PP28): Evolutionary Convolutional Neural Network for High Energy Physics Detector Simulation

Sofia Vallecorsa (CERN)

High Energy Physics relies on Monte Carlo (MC) for different aspects of data analysis. MC simulation implement complex computations that, today, result in ~50% of CERN Computing Grid resources. Several alternative approaches are being investigated trading some accuracy for speed. Deep Learning approaches, for example, can result in x3000 speed-up while retaining 10% accuracy with respect to MC.

Design and optimisation of neural networks is very difficult and time consuming. Evolutionary computing could be exploited to improve this process, while providing the benefit of both network training and topology optimization in one step. By coding a neural network into genes and chromosome, Genetic Algorithms (GA) would exhibit numerous advantages: easily parallelizable, they could help reach global instead of local optima often selected by Stochastic Gradient Descent (SGD); they could also be combined to SGD for fine tuning.

Our project intends to use GA to train and optimise a 3-dimensional Convolutional Generative Adversarial Network we have developed for particle detector simulation. It is implemented in a few steps: a first phase, will implement a simplified version of our GAN network, focusing on one of the two networks that constitute the GAN (the “discriminator”). We will design a first prototype and define the method applicability (in terms of network complexity and computing resources). We will gradually increase the complexity of the problem, in terms of input image size and network features and finally implement the full adversarial training approach. We will compare performances to standard SGD and classical optimisation approaches (i.e. Bayesian).

(PP29): Cygnus: A Multi-Hybrid Supercomputing Platform with GPUs and FPGAs
Taisuke Boku (University of Tsukuba)

Graphics processing units (GPUs) have been widely used in high-performance computing (HPC) systems as accelerators because they can offer good peak performance and high memory bandwidth. However, the GPU is not almighty as an accelerator because it is not effective in applications that employ complicated algorithms using exception, non single-instruction-multiple-data streams (SIMD), partially poor parallelism, etc. To address these problems, field programmable gate arrays (FPGAs) have gained attention in HPC research because their computation and communication capabilities have dramatically improved in recent years as a result of improvements to semiconductor integration technologies that depend on Moore's Law. In addition to FPGA performance improvements, OpenCL-based FPGA development toolchains have been developed and offered by FPGA vendors, which reduces the programming effort required as compared to the past, and as a result, the interest in the FPGA from HPC field has been more increased. In this project, we make FPGAs cooperate with GPUs and utilize both accelerators complementarily in order to maximize the FPGA potential and to apply it to GPU-based HPC systems. We propose how to use FPGA for HPC which enables on-the-fly offloading computation at which CPUs/GPUs perform poorly to FPGAs while performing low-latency intra/inter-node

communication, build a programming framework to comprehensively control these functionalities from the CPU, and demonstrate the effectiveness of our proposed approach by applying it to computational science applications.

(PP30): Deep Learning for Satellite Imagery

Sofia Vallecorsa (CERN)

Our project is a unique partnership between CERN, Intel, and the United Nations Institute for Training and Research (UNITAR) to use Deep Learning (DL) to improve the analysis of optical satellite imagery for humanitarian purposes. The core objective is to create spectrally valid simulated high-resolution satellite imagery depicting humanitarian situations such as refugee settlements, flood conditions, damaged infrastructure, and more, by using techniques such as Generative Adversarial Networks (GANs). UNITAR hosts the UN Operational Satellite Applications Centre (UNOSAT), which uses satellite imagery to support disaster response, humanitarian operations, and other activities of the broader UN system. UNITAR has in recent years started studying the application of DL to satellite imagery analysis, in order to improve efficiency in the many manual tasks frequently required: for example, digitizing a refugee settlement in a satellite image can take many hours, sometimes days of effort. Mapping displaced persons across broad regions such as northwest Syria can in turn be weeks of work. DL methods could greatly reduce the amount of time needed to complete such tasks: a key factor to an effective deployment of field operations in critical humanitarian situations. High-resolution satellite imagery is often licensed in such a way that it can be difficult to share it across UNITAR, UN partners, and academic organizations, reducing the amount of data available to train DL models. This fact has inhibited UNITARs DL research possibilities in various ways. The creation of realistic and spectrally accurate simulated images could enable and stimulate data sharing.

Research Paper

(back to top)

Monday, June 17th

Room: Panorama 1
4:00 pm - 6:00 pm

Research Paper (Award) Session 01

Session Description: The following awards will be given to outstanding research papers submitted to the conference: HANS MEUER AWARD The Hans Meuer Award honors the most outstanding research paper submitted to the conference's Research Papers Committee. This award has been introduced in the memory of the late Dr. Hans Meuer, general chair of the ISC conference from 1986 through 2014, and co-founder of the TOP500 project. From all submitted research papers, the Research Papers Committee will select the overall best paper for the award. GAUSS AWARD The GCS Award honors the most outstanding research paper submitted to the Research Papers Committee in the field of HPC. The GCS Award has been a key component of the conference each year since the foundation of the Gauss Centre for Supercomputing (GCS) in 2008. It is sponsored by GCS, an alliance of Germany's three national supercomputing centers — the High-Performance Computing Center Stuttgart (HLRS), Jülich Supercomputing Centre (JSC), and Leibniz Supercomputing Centre (LRZ).

Introduction Award Session
Yutong Lu, Carsten Trinitis

Hans Meuer Award Finalist 1: GPUMixer: Performance-Driven Floating-Point Tuning for GPU Scientific Applications
Ignacio Laguna (Lawerence Livermore National Laboratory)

We present GPUMixer, a tool to perform mixed-precision floating-point tuning on scientific GPU applications. While precision tuning techniques are available, they are designed for serial programs and are accuracy-driven, i.e., they consider configurations that satisfy accuracy constraints, but these

configurations may degrade performance. GPUMixer, in contrast, presents a performance-driven approach for tuning. We introduce a novel static analysis that finds Fast Imprecise Sets (FISets), sets of operations on low precision that minimize type conversions, which often yield performance speedups. To estimate the relative error introduced by GPU mixed-precision, we propose shadow computations analysis for GPUs, the first of this class for multi-threaded applications. GPUMixer obtains performance improvements of up to 46.4% of the ideal speedup in comparison to only 20.7% found by state-of-the-art methods.

Hans Meuer Award Finalist 2: Global Task Data Dependencies in PGAS Applications
Joseph Schuchart (Universität Stuttgart, Höchstleistungsrechenzentrum Stuttgart)

Recent years have seen the emergence of two independent programming models challenging the traditional two-tier combination of message passing and thread-level work-sharing: partitioned global address space (PGAS) and task-based concurrency. In the PGAS programming model, synchronization and communication between processes are decoupled, providing significant potential for reducing communication overhead. At the same time, task-based programming allows to exploit a large degree of shared-memory concurrency. The inherent lack of fine-grained synchronization in PGAS can be addressed through fine-grained task synchronization across process boundaries. In this work, we propose the use of task data dependencies describing the data-flow in the global address space to synchronize the execution of tasks created in parallel on multiple processes. We present a description of the global data dependencies, describe the necessary interactions between the distributed scheduler instances required to handle them, and discuss our implementation in the context of the DASH C++ PGAS framework. We evaluate our approach using the Blocked Cholesky Factorization and the LULESH proxy app, demonstrating the feasibility and scalability of our approach.

GCS Award Winning Paper: End-to-end Resilience for HPC Applications
Frank Mueller (NCSU)

A plethora of resilience techniques have been investigated ranging from checkpoint/restart over redundancy to algorithm-based fault tolerance. Each technique works well for a different subset of application kernels, and depending on the kernel, has different overheads, resource requirements, and fault masking capabilities. If, however, such techniques are combined and they interact across kernels, new vulnerability windows are created. This work contributes the idea of end-to-end resilience by protecting windows of vulnerability between kernels guarded by different resilience techniques. It introduces the live vulnerability factor (LVF), a new metric that quantifies any lack of end-to-end protection for a given data structure. The work further promotes end-to-end application protection across kernels via a pragma-based specification for diverse resilience schemes with minimal programming effort. This lifts the data protection burden from application programmers allowing them to focus solely on algorithms and performance while resilience is specified and subsequently embedded into the code

through the compiler/library and supported by the runtime system. Two case studies demonstrate that end-to-end resilience meshes well with different execution paradigms and assess its overhead and effectiveness for different codes. In experiments with case studies and benchmarks, end-to-end resilience has an overhead over kernel-specific resilience of less than 3% on average and increases protection against bit flips by a factor of three to four.

Tuesday, June 18th

Room: Analog 1, 2
8:30 am - 10:00 am

Research Paper Session - Machine Learning and Emerging Technologies

Layout-Aware Embedding for Quantum Annealing Processors
Jose P. Pinilla (University of British Columbia)

Due to the physical limit in connectivity between qubits in Quantum Annealing Processors (QAPs), when sampling from a problem formulated as an Ising graph model, it is necessary to embed the problem onto the physical lattice of qubits. A valid mapping of the problem nodes into qubits often requires qubit chains to ensure connectivity.

We introduce the concept of layout-awareness for embedding; wherein information about the layout of the input and target graphs is used to guide the allocation of qubits to each problem node. We then evaluate the consequent impact on the sampling distribution obtained from D-Wave's QAP, and provide a set of tools to assist developers in targeting QAP architectures using layout-awareness. We quantify the results from a layout-agnostic and a layout-aware embedding algorithm on (a) the success rate and time at finding valid embeddings, (b) the metrics of the resulting chains and interactions, and (c) the energy profile of the annealing samples. The latter results are obtained by running experiments on a D-Wave Quantum Annealer, and are directly related to the ability of the device to solve complex problems.

Our technique effectively reduces the search space, which improves the time and success rate of the embedding algorithm and/or finds mappings that result in lower energy samples from the QAP. Together, these contributions are an important step towards an understanding of how near-future Computer-Aided Design (CAD) tools can work in concert with quantum computing technologies to solve previously intractable problems.

Densifying Assumed-sparse Tensors: Improving Memory Efficiency and MPI Collective

Performance during Tensor Accumulation for Parallelized Training of Neural Machine Translation Models

Lucas A. Wilson (Dell EMC)

Neural machine translation - using neural networks to translate human language - is an area of active research exploring new neuron types and network topologies with the goal of dramatically improving machine translation performance. Current state-of-the-art approaches, such as the multi-head attention-based transformer, require very large translation corpuses and many epochs to produce models of reasonable quality. Recent attempts to parallelize the official TensorFlow "Transformer" model across multiple nodes have hit roadblocks due to excessive memory use and resulting out of memory errors when performing MPI collectives.

This paper describes modifications made to the Horovod MPI-based distributed training framework to reduce memory usage for transformer models by converting assumed-sparse tensors to dense tensors, and subsequently replacing sparse gradient gather with dense gradient reduction. The result is a dramatic increase in scale-out capability, with CPU-only scaling tests achieving 91% weak scaling efficiency up to 1200 MPI processes (300 nodes), and up to 65% strong scaling efficiency up to 400 MPI processes (200 nodes) using the Stampede2 supercomputer.

Learning Neural Representations for Predicting GPU Performance

Shweta Salaria (Tokyo Institute of Technology, AIST-Tokyo Tech RWBC-OIL)

The graphic processing units (GPUs) have become a primary source of heterogeneity in today's computing systems. With the rapid increase in number and types of GPUs available, finding the best hardware accelerator for each application is a challenge. For that matter, it is time consuming and tedious to execute every application on every GPU system to learn the correlation between application properties and hardware characteristics. To address this problem, we extend our previously proposed collaborating filtering based modeling technique, to build an analytical model which can predict performance of applications across different GPU systems. Our model learns representations, or embeddings (dense vectors of latent features) for applications and systems and uses them to characterize the performance of various GPU-accelerated applications. We improve state-of-the-art collaborative filtering approach based on matrix factorization by building a multi-layer perceptron. In addition to increased accuracy in predicting application performance, we can use this model to simultaneously predict multiple metrics such as rates of memory access operations. We evaluate our approach on a set of 30 well-known micro-applications and seven Nvidia GPUs. As a result, we can predict expected instructions per second value with 90.6% accuracy in average.

Room: Analog 1, 2
11:00 am - 12:30 pm

Research Paper Session - Data Storage and Visualisation

A Near-Data Processing Server Architecture and Its Impact on Data Center Applications

Tao Xie (San Diego State University)

Existing near-data processing (NDP) techniques have demonstrated their strength for some specific data-intensive applications. However, they might be inadequate for a data center server, which normally needs to perform a diverse range of applications from data-intensive to compute-intensive. How to develop a versatile NDP-powered server to support various data center applications remains an open question. Further, a good understanding of the impact of NDP on data center applications is still missing. For example, can a compute-intensive application also benefit from NDP? Which type of NDP engine is a better choice, an FPGA-based engine or an ARM-based engine? To address these issues, we first propose a new NDP server architecture that tightly couples each SSD with a dedicated NDP engine to fully exploit the data transfer bandwidth of an SSD array. Based on the architecture, two NDP servers ANS (ARM-based NDP Server) and FNS (FPGA-based NDP Server) are introduced. Next, we implement a single-engine prototype for each of them. Finally, we measure performance, energy efficiency, and cost/performance ratio of six typical data center applications running on the two prototypes. Some new findings have been observed.

Comparing the Efficiency of In Situ Visualization Paradigms at Scale

James Kress (Oak Ridge National Laboratory, University of Oregon)

This work compares the two major paradigms for doing in situ visualization: in-line, where the simulation and visualization share the same resources, and in-transit, where simulation and visualization are given dedicated resources. Our runs vary many parameters, including simulation cycle time, visualization frequency, and dedicated resources, to study how tradeoffs change over configuration. In particular, we consider simulations as large as 1,024 nodes (16,384 cores) and dedicated visualization resources with as many as 512 nodes (8,192 cores). We draw conclusions about when each paradigm is superior, such as in-line being superior when the simulation cycle time is very fast. Surprisingly, we also find that in-transit can minimize the total resources consumed for some configurations, since it can cause the visualization routines to require fewer overall resources when they run at lower concurrency. For example, one of our scenarios finds that allocating 25% more resources for visualization allows the simulation to run 61% faster than its in-line comparator. Finally, we explore various models for quantifying the cost for each paradigm, and consider transition points when one paradigm is superior to the other. Our contributions inform design decisions for simulation scientists when performing in situ visualization.

SLOPE: Structural Locality-aware Programming Model for Composing Array Data Analysis
Kesheng Wu (Lawrence Berkeley National Lab)

MapReduce brought on the Big Data revolution. However, its impact on scientific data analyses has been limited because of fundamental limitations in its data and programming models. Scientific data is typically stored as multidimensional arrays, while MapReduce is based on key-value (KV) pairs. Applying MapReduce to analyze array-based scientific data requires a conversion of arrays to KV pairs. This conversion incurs a large storage overhead and loses structural information embedded in the array. For example, analysis operations, such as convolution, are defined on the neighbors of an array element. Accessing these neighbors is straightforward using array indexes, but requires complex and expensive operations like self-join in the KV data model. In this work, we introduce a novel 'structural locality'-aware programming model (SLOPE) to compose data analysis directly on multidimensional arrays. We also develop a parallel execution engine for SLOPE to transparently partition the data, to cache intermediate results, to support in-place modification, and to recover from failures. Our evaluations with real applications show that SLOPE is over ninety thousand times faster than Apache Spark and is 38% faster than TensorFlow.

Room: Analog 1, 2
1:45 pm - 3:15 pm

Research Paper Session - Performance Modelling and Measurement & Algorithms

PerfMemPlus: A Tool for Automatic Discovery of Memory Performance Problems
Christian Helm (The University of Tokyo)

In high-performance computing many performance problems are caused by the memory system. Because such performance bugs are hard to identify, analysis tools play an important role in performance optimization. Today's processors offer feature-rich performance monitoring units with support for instruction sampling but existing tools only partially use this data. Previously, performance counters were used to measure the memory bandwidth. But the attribution of high bandwidth to source code has been difficult and imprecise. We introduce a novel method for identifying performance degrading bandwidth usage and attributing it to specific objects and source code lines. This paper also introduces a new method for false sharing detection. It can differentiate false and true sharing, identify objects and source code lines where the accesses to falsely shared objects are happening. It can uncover false sharing, which has been overlooked by previous tools. PerfMemPlus automatically reports those issues by using instruction sampling data captured with a single profiling run. This simplifies the tedious search for the location of performance problems in complex code. The tool design is simple, provides support for many

existing and upcoming processors and the recorded data can be easily used in future research. We show that PerfMemPlus can automatically report performance problems without producing false positives. Additionally, we present case studies that show how PerfMemPlus can pinpoint memory performance problems in the PARSEC benchmarks and machine learning applications.

Performance Exploration Through Optimistic Static Program Annotations
Johannes Doerfert (Argonne National Laboratory)

Compilers are limited by the static information directly or indirectly encoded in the program. Low-level languages, such as C/C++, are considered problematic as their weak type system and relaxed memory semantic allows for various, sometimes non-obvious, behaviors. Since compilers have to preserve the program semantics for all program executions, the existence of exceptional behavior can prevent optimizations that the developer would consider valid and might expect. Analyses to guarantee the absence of disruptive and unlikely situations are consequently an indispensable part of an optimizing compiler. However, such analyses have to be approximative and limited in scope as global and exact solutions are infeasible for any non-trivial program.

In this paper, we present an automated tool to measure the effect missing static information has on the optimizations applied to a given program. The approach generates an optimistically optimized program version which, compared to the original, defines a performance gap that can be closed by better compiler analyses and selective static program annotations.

Our evaluation on six already tuned proxy applications for high-performance codes shows speedups of up to 20.6%. This clearly indicates that static uncertainty limits performance. At the same time, we observed that compilers are often unable to utilize additional static information. Thus, manual annotation of all correct static information is therefore not only error prone but also mostly redundant.

Toward efficient architecture-independent algorithms for dynamic programs
Zafar Ahmad (Stony Brook University)

We argue that the recursive divide-and-conquer paradigm is highly suited for designing algorithms to run efficiently under both shared-memory (multi- and manycores) and distributed-memory settings. The depth-first recursive decomposition of tasks and data is known to allow computations with potentially high temporal locality, and automatic adaptivity when resource availability (e.g., available space in shared caches) changes during runtime. Higher data locality leads to better intra-node I/O and cache performance and lower inter-node communication complexity, which in turn can reduce running times and energy consumption. Indeed, we show that a class of grid-based parallel recursive divide-and-conquer algorithms (for dynamic programs) can be run with provably optimal or near-optimal performance bounds on fat cores (cache complexity), thin cores (data movements), and purely distributed-memory machines

(communication complexity) without changing the algorithm's basic structure. Two-way recursive divide-and-conquer algorithms are known for solving dynamic programming problems on shared-memory multicore machines. We show how to extend them to run efficiently also on manycore GPUs and distributed-memory machines. Our GPU algorithms work efficiently even when the data is too large to fit into the host RAM. These are external-memory algorithms based on recursive r-way divide and conquer, where r (≥ 2) varies based on the current depth of the recursion. Our distributed-memory algorithms are also based on multi-way recursive divide and conquer that extends naturally inside each shared-memory multicore/manycore compute node. We show that these algorithms are work-optimal and have low latency and bandwidth bounds. We also report empirical results for our GPU and distribute memory algorithms.

Room: Panorama 2
5:00 pm - 5:15 pm

Hans Meuer Award Ceremony

Session Description: The Hans Meuer Award honors the most outstanding research paper submitted to the conference's Research Papers Committee. This award has been introduced in the memory of the late Dr. Hans Meuer, general chair of the ISC conference from 1986 through 2014, and co-founder of the TOP500 project.

Wednesday, June 19th

Room: Substanz 1, 2
8:30 am - 9:30 am

Research Paper Session - HPC Applications

MaLTESE: Large-Scale Simulation-Driven Machine Learning for Transient Driving Cycles
Shashi M. Aithal (Argonne National Laboratory)

Optimal engine operation during a transient driving cycle is the key to achieving greater fuel economy and reduced emissions. A large-scale simulation-driven machine-learning approach is presented in this work to explore the parameter space for optimal engine performance and emissions. A parallel, fast, robust, physics-based reduced-order engine simulator is used to obtain performance and emission characteristics of engines over a wide range of control parameters under various transient driving

conditions (drive cycles). We scale the simulation up to 3,096 nodes of the Theta supercomputer at the Argonne Leadership Computing Facility to generate data required to train a machine learning model. The trained model is then used to predict various engine parameters of interest and compared with results predicted by the engine. Our results show that a deep neural-network- based surrogate model achieves a high accuracy: Pearson product-moment cor- relation coefficient values larger than 0.99 and mean absolute percentage error within 1.07% for various engine parameters such as exhaust temperature, exhaust pressure, nitric oxide, and engine torque. Once trained, the deep-neural-network- based surrogate-model is fast for inference: it requires about 16 microseconds for predicting the engine performance and emissions for a single design configuration as compared with about 0.5 second per configuration with the engine simulator. Moreover, we demonstrate that transfer learning and retraining can be leveraged to incrementally retrain the surrogate model to cope with new configurations that falls outside the training data space.

Petaflop Seismic Simulations in the Public Cloud
Alexander Heinecke (Intel)

During the last decade cloud services became a popular solution for diverse applications. Additionally, hardware support for virtualization closed performance gaps, compared to on-premises, bare-metal systems. This development is driven by offloaded hypervisors and full CPU virtualization. Today's cloud service providers, such as Amazon or Google, offer the ability to assemble application-tailored clusters to maximize performance. However, from an interconnect point of view, one has to tackle a 4-5$\times$ slow-down in terms of bandwidth and 30$\times$ in terms of latency, compared to latest high-speed and low-latency interconnects. Taking into account the high per-node and accelerator-driven performance of latest supercomputers, we observe that the network-bandwidth performance of recent cloud offerings is within 2$\times$ of large supercomputers. In order to address these challenges, we present a comprehensive application-centric approach for high-order seismic simulations utilizing the ADER discontinuous Galerkin finite element method. This covers the tuning of the operating system, micro-benchmarking, and finally, the efficient execution of our solver in the cloud. Due to this performance-oriented end-to-end workflow, we were able to achieve 1.09 PFLOPS on 768 AWS c5.18xlarge instances, offering 27,648 cores with 5 PFLOPS of theoretical computational power. This correlates to an achieved peak efficiency of over 20\% and a close-to 90\% parallel efficiency in a weak scaling setup. In terms of strong scalability, we were able to strong-scale a science scenario from 2 to 64 instances with 60\% parallel efficiency. This work is, to the best of our knowledge, the first of its kind at such a large scale.

Room: Substanz 1, 2
11:00 am - 12:30 pm

Research Paper Session - Programming Models & System Software, Architectures & Networks

Resilient Optimistic Termination Detection for the Async-Finish Model

Sara Hamouda (INRIA)

Driven by increasing core count and decreasing mean-time-to-failure in supercomputers, HPC runtime systems must improve support for dynamic task-parallel execution and resilience to failures. The async-finish task model, adapted for distributed systems as the asynchronous partitioned global address space programming model, provides a simple way to decompose a computation into nested task groups, each managed by a 'finish' that signals the termination of all tasks within the group.

For distributed termination detection, maintaining a consistent view of task state across multiple unreliable processes requires additional book-keeping when creating or completing tasks and finish-scopes. Runtime systems which perform this book-keeping pessimistically, i.e. synchronously with task state changes, add a high communication overhead compared to non-resilient protocols. In this paper, we propose optimistic finish, the first message-optimal resilient termination detection protocol for the async-finish model. By avoiding the communication of certain task and finish events, this protocol allows uncertainty about the global structure of the computation which can be resolved correctly at failure time, thereby reducing the overhead for failure-free execution.

Performance results using micro-benchmarks and the LULESH hydrodynamics proxy application show significant reductions in resilience overhead with optimistic finish compared to pessimistic finish. Our optimistic finish protocol is applicable to any task-based runtime system offering automatic termination detection for dynamic graphs of non-migratable tasks.

Finepoints: Partitioned Multithreaded MPI Communication

Ryan E. Grant (Sandia National Laboratories, University of New Mexico)

The MPI multithreading model has been historically difficult to optimize; the interface that it provides for threads was designed as a process-level interface. This model has led to implementations that treat function calls as critical regions and protect them with locks to avoid race con- ditions. We hypothesize that an interface designed specifically for threads can provide superior performance than current approaches and even outperform single-threaded MPI.

In this paper, we describe a design for partitioned communication in MPI that we call finepoints. First, we assess the existing communication models for MPI two-sided communication and then introduce finepoints as a hybrid of MPI models that has the best features of each existing MPI communciation model. In addition, "partitioned communication" created with finepoints leverages new network hardware

features that cannot be exploited with current MPI point-to-point semantics, making this new approach both innovative and useful both now and in the future.

To demonstrate the validity of our hypothesis, we implement a finepoints library and show improvements against a state-of-the-art multithreaded optimized Open MPI implementation on a Cray XC40 with an Aries network. Our experiments demonstrate up to a 12× reduction in wait time for com- pletion of send operations. This new model is shown working on a nuclear reactor physics neutron-transport proxy-application, providing up to 26.1% improvement in communication time and up to 4.8% improvement in runtime over the best performing MPI communication mode, single-threaded MPI.

Evaluating Quality of Service Traffic Classes on the Megafly Network
Neil McGlohon (Rensselaer Polytechnic Institute)

An emerging trend in High Performance Computing (HPC) systems that use hierarchical topologies (such as dragonfly) is that the applications are increasingly exhibiting high run-to-run performance variability. This poses a significant challenge for application developers, job schedulers, and system maintainers. One approach to address the performance variability is to use newly proposed network topologies such as megafly (or dragonfly+) that offer increased path diversity compared to a traditional fully connected dragonfly. Yet another approach is to use quality of service (QoS) traffic classes that ensure bandwidth guarantees.

In this work, we select HPC application workloads that have exhibited performance variability on current 2-D dragonfly systems. We evaluate the baseline performance expectations of these workloads on megafly and 1-D dragonfly network models with comparably similar network configurations. Our results show that the megafly network, despite using fewer virtual channels (VCs) for deadlock avoidance than a dragonfly, performs as well as a fully connected 1-D dragonfly network. We then exploit the fact that megafly networks require fewer VCs to incorporate QoS traffic classes. We use bandwidth capping and traffic differentiation techniques to introduce multiple traffic classes in megafly networks. In some cases, our results show that QoS can completely mitigate application performance variability while causing minimal slowdown to the background network traffic.

Research Poster

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Tuesday, June 18th

Room: Substanz 1, 2
8:30 am - 10:00 am

Research Posters Session

Introduction Research Posters Session
Sunita Chandrasekaran (University of Delaware), Ryusuke Egawa (Tohoku University)

(RP01) CPU Water Cooling Temperature Effects on the Performance and Energy Consumption
Jorji Nonaka (RIKEN R-CCS)

Energy efficiency has become one of the critical element for data center operation. Recently, hot water cooling technology is famous as an approach to reduce power consumption for cooling and to improve PUE (Power Usage Effectiveness). In the hot water cooling, since the cooling water temperature is higher than the outside air temperature, a part or all of the exhaust heat is naturally cooled by the outside air. Therefore, it is possible to reduce power consumption for cooling. On the other hand, recent Intel architecture based CPU has a mechanism to automatically lower the clock frequency when it gets hot to prevent thermal runaway and failure. And in general, the power consumption of the CPU increases as the CPU temperature becomes higher as the leakage current increases. To fairly evaluate the effectiveness of the hot water cooling from the viewpoint of energy efficiency, the effect of increasing the power consumption of the CPU, the impact on degrading the performance and the effect of lowering the power consumption for cooling is needed to take into consideration. In this poster, we try to evaluate the impact of increasing the power consumption of the CPU and the impact on degrading the performance qualitatively and systematically by investigating the change in sustained performance and power consumption when CPU cooling water temperature changes.

(RP02) DEEP: Hybrid Approach for Deep Learning
Valentin Kozlov (Karlsruhe Institute of Technology (KIT))

The DEEP-HybridDataCloud project researches on intensive computing techniques such as deep learning, that require specialized GPU hardware to explore very large datasets, through a hybrid-cloud approach that enables the access to such resources. DEEP is built on User-centric policy, i.e. we understand the needs of our user communities and help them to combine their services in a way that encapsulates technical details the end user does not have to deal with. DEEP takes care to support users of different levels of experience by providing different integration paths. We show our current solutions to the problem, which among others include the Open Catalog for deep learning applications, DEEP-as-a-Service API for providing web access to machine learning models, CI/CD pipeline for user applications, Testbed resources. We also present our use-cases tackling various problems by means of deep learning and serving to demonstrate usefulness and scalability of our approach.

(RP03) Design of an FPGA-based Matrix Multiplier with Task Parallelism

Yiyu Tan (RIKEN Center for Computational Science)

Matrix multiplication is one of the fundamental building blocks of linear algebra. It requires computer systems have huge computing capability as problem size is increased. In this research, an FPGA-based matrix multiplier with task parallelism is designed and implemented by using the FPGA board DE5a-NET. The matrix multiplier is based on the systolic array architecture with 10 × 16 processing elements, all modules except the data loading modules are autorun to hide computation overhead, and data of matrix A are shifted from left to right while data of matrix B are moved from top to bottom in the systolic array to reuse data. After implementation by using FPGA, the proposed matrix multiplier utilizes more DSP blocks and achieves much higher clock frequency over the Intel's OpenCL example with data parallelism on FPGA. When data are single-precision floating-points, the proposed matrix multiplier averagely achieves about 785 GFLOPs in computation throughput and 81 GFLOPs/W in energy efficiency. Compared with the Intel's OpenCL example with data parallelism on FPGA, software simulations based on the Intel MKL and OpenBLAS libraries, the proposed matrix multiplier averagely outperforms by 3.2 times, 1.3 times, and 1.6 times in computation throughput, and by 3.4 times, 12.7 times, and 14.6 times in energy efficiency, respectively, even if the fabrication technology of FPGA is 20 nm while it is 14 nm in CPU.

(RP04) Distributed Deep Learning with FPGA Ring Allreduce

Kenji Tanaka (NTT Corporation, NTT Device Technology Laboratories)

Among various methods for efficient distributed Deep Learning (DL), the top three state-of-the-art ImageNet/ResNet-50 training were achieved by utilizing a distributed data-parallel DL with Ring Allreduce or 2D-Torus Allreduce. However, it is difficult to apply them at large scale because latency is accumulated at each node due to data moving to GPU or CPU for Reduce processes. Our solution is to use In-Network Computing to handle data reduction while it is being transferred in the network. Since the conventional In-Network Computing system can apply to only hierarchical Allreduce, in this work, we

propose a new In-Network Computing system that can support Ring Allreduce. In order to minimize communication overhead, we apply layer-based computing/communication overlap and optimize it for our proposed In-Network Computing system. We also propose a highly productive software stack consisting of a DL framework and heterogeneous device control languages. The evaluation results show that we can reduce the communication overhead by 84.27% at a batch size of 32 without any accuracy degradation. Moreover, the total learning time can be reduced by 7% when using 4 nodes learning system. It is confirmed that our system can significantly reduce the communication overhead without deteriorating accuracy when applying to a large-scale distributed DL with a large communication load. Although the current top data is 2-D Torus Allreduce using ASIC in domain specific architecture, the result shows that the communication overhead is shorter by applying the proposed system, which indicates the possibility of In-Network Computing.

(RP05) ENEA CRESCO HPC Clusters: A Working Example of a Multifabric GPFS Spectrum Scale Layout

Francesco Iannone (ENEA)

ENEA is the Italian National Agency for New Technologies, Energy and Sustainable Economic Development. ENEA operates in many sectors among which the most important are: energy technologies, materials physics, life sciences and climate. In the framework of its institutional mission, the ICT Division provides computing and storage resources integrated into ENEAGRID/CRESCO, an infrastructure distributed over 6 sites, whose main facilities are the HPC CRESCO clusters. The bulk of all storage is based on IBM Spectrum Scale (GPFS) since many years. The access to data, even over WAN, is managed by GPFS clusters. In May 2018 the new cluster CRESCO6 was inaugurated. CRESCO6, a 1.4 Pflops based on Intel Xeon X86_64 SkyLake CPU ranked 420th of TOP 500 Nov.2018 list. While the interconnection of CRESCO6 is based on Intel Omni-Path (OPA) (100 Gbps), the previous CRESCO4 and CRESCO5 clusters have a network based on InfniBand QDR Truescale fabric (40 Gbps). Hence, in order to provides storage to all CRESCO clusters a GPFS multifabric layout has been implemented after dedicated tests. The work describes the ENEAGRID/CRESCO infrastructure and in particular the solution adopted to implement the GPFS multifabric, and the next future developments.

(RP06) Reduction Operations on Modern Supercomputers: Challenges and Solutions

Hari Subramoni (The Ohio State University)

Message Passing Interface (MPI) is the dominant parallel programming model offering various primitives like point-to-point and collectives. MPI Allreduce is a very popular collective used in the scientific/DL applications. While scientific applications typically use small/medium messages, DL applications need large message reductions. On the other hand, advances in processor and interconnect technologies brings about novel techniques that have the potential to improve the performance. Here the broad challenge is how do we design high-performance reduction collectives that take advantage of the trends

in modern processor architecture to deliver good performance for reduction for various message sizes. In this work, we take up this challenge and use various optimizations like network offload mechanisms, efficient pipelining, and zero-copy intra-node communication to propose three designs each targeting three ranges of message sizes. The evaluation of the proposed designs shows significant performance on a wide variety of microbenchmarks and scientific and DL applications.

(RP07) Towards Clean Propulsion with Synthetic Fuels: A Cluster-Modularized Approach Employing Hierarchies of Simulations and Deep Learning

Mathis Bode (Institute for Combustion Technology, RWTH Aachen University)

Development of new clean propulsion technology is difficult as the parameter space of possible realizations is large and cannot be investigated cost efficiently by experimental methods as, for example, geometry optimizations require manufacturing. The only way to overcome this issue is by combining experimental and simulation techniques. However, also simulation techniques struggle with the wide range of involved scales, and a direct approach would exceed the currently available computing capacities. Therefore, this work presents a hierarchical simulation approach employing high-order models (DNS) as well as reduced-order models (LES) utilized on different German supercomputer. While the used high-order models naturally rely on all-to-all communication, the reduced-order models mostly require local communication. Consequently, the DNS were performed on JUQUEEN with its 5D torus network and the LES on Hazel Hen. As the data of the DNS are required as BC for the LES, coupling is needed. In this work, a CNN was trained with the DNS data in order to reduce the required data transfer from TBs to GBs. This training was done using modularized computing on JUQUEEN/JURECA with on-the-fly data streaming. In this way, JURECA's GPUs were efficiently used and classical I/O avoided. Pre- and postprocessing was done on CLAIX16. The optimal cluster choices enabled very good scaling and node performance. Overall, the combination of hierarchical simulations, modularized computing and deep learning allowed an iterative technology development cycle, as feedback to the experiment was possible on time (edge2cloud). Optimizations with respect to nozzle geometry, injection conditions and fuel properties were realized.

(RP08) News from Black Holes in Star Clusters Simulated with Large GPU Clusters

Francesco Paolo Rizzuto (Max Planck Institute for Astrophysics (Garching))

We use the newly developed direct N-body integrator Nbody6++GPU to simulate the evolution of globular clusters with a high level of realism. We follow the dynamical and stellar evolution of individual and binary stars, their evolution into neutron stars and black holes, interactions, dynamical binary formation, and mergers. To accomplish this, Nbody6++GPU is parallelised using hybrid methods (MPI, GPU, OpenMP, and AVX/SSE) and reaches high performance for accurate gravity computation. Nbody6++GPU has been used to compute the largest GC simulation so far, with one million stars. We present scaling and performance properties of the gravity calculation on multi-GPU systems and different single GPUs:

Kepler K20, Pascal P100, and Volta V100. In a scientific application, we study the formation of intermediate-mass black holes in globular star clusters, growing to more than a few hundred solar masses by interactions and mergers with other stars and stellar black holes. Typical formation paths are presented for simulations carried out at the newly installed COBRA GPU system of the Max Planck Computing & Data Facility in Garching.

(RP09) Accelerating Chemical Shift Prediction for Large-scale Biomolecular Modeling
Sunita Chandrasekaran (University of Delaware)

Experimental chemical shifts (CS) from solution and solid state magic-angle-spinning nuclear magnetic resonance spectra provide atomic level data for each amino acid within a protein or complex. However, structure determination of large complexes and assemblies based on NMR data alone remains challenging due to the complexity of the calculations. Here, we present a hardware accelerated strategy for the estimation of NMR chemical-shifts of large macromolecular complexes. We demonstrate the feasibility of our approach in systems of increasing complexity ranging from 2,000 to 11,000,000 atoms.

The scope of this project is the acceleration of a code known as PPM_One onto parallel hardware such as GPUs. The original code was not intended to function on a parallel architecture and was not optimized enough to realistically compute the estimated chemical shift of these large complexes. The best result we achieved was a 67x speedup when comparing the single core performance of the code versus a single Volta V100 GPU. This is not considering the overall speedup over the original, unoptimized code. Now, using GPU acceleration, a code that was taking upwards of 2.5 hours on large datasets can be completed in just over 2 minutes. Also, with the same code targeting an Intel multicore CPU, with 32 cores, we are seeing a 22x speedup versus the single core runtime. A future outlook for this project would be to incorporate some of these accelerated molecular dynamics functions into other code bases, such as the NAMD project.

(RP10) High-Performance Computing of Thin QR Decomposition on Parallel Systems
Takeshi Terao (Shibaura Institute of Technology)

This poster aims to propose the preconditioned Cholesky QR algorithms for thin QR decomposition (also called economy size QR decomposition). CholeskyQR is known as a fast algorithm employed for thin QR decomposition, and CholeskyQR2 is recently proposed for improving the orthogonality of a Q-factor computed by CholeskyQR. Although such Cholesky QR algorithms can efficiently be implemented in high-performance computing environments, they are not applicable for ill-conditioned matrices, as compared to the Householder QR and the Gram-Schmidt algorithms. To address this problem, we propose two algorithms named LU-Cholesky QR and Robust Cholesky QR. On LU-Chlesky QR, we apply the concept of LU decomposition to the Cholesky QR algorithms, i.e., the idea is to use LU-factors of a given matrix as preconditioning before applying Cholesky decomposition. Robust Cholesky QR uses a

part of Cholesky factor for constructing the preconditioner when Cholesky decomposition breaks down. The feature of Robust Cholesky QR is its adaptiveness for difficulty of problems. In fact, the cost for the preconditioning in Robust Cholesky QR can be omitted if a given matrix is moderately well-conditioned. Numerical examples provided in this poster illustrate the efficiency of the proposed algorithms in parallel computing on distributed memory computers.

(RP11) HPC Oriented Algorithm for Computation of Recurrence Quantitative Analysis

Tomáš Martinovič (IT4Innovations, VŠB - Technical University of Ostrava)

Recurrence quantitative analysis (RQA) is a quantification of the dynamical properties of time series. This method is used in many medicine, biology, speech and vocalization research. The main drawback of this method is its computational complexity. The first step for the RQA is the computation of the distance matrix of subsequences of the time series. Afterwards, this distance matrix is thresholded, setting 1 if the distance is less than a parameter ε and 0 otherwise. These are called recurrence plots. The histogram of consecutive 1s on the diagonals is computed. This histogram is then used to compute RQA. We present an algorithm for the computation of RQA directly from the input data. This algorithm allows easy parallelization of the computation with minimal spatial complexity.

(RP12) A Container-Based Approach to HPC Cloud

Guohua Li (KISTI/Korea National Supercomputing Center)

Recently, the VM-based HPC service has been provided in the cloud environment to satisfy portability, flexibility, scalability, and reduction of deployment costs in the HPC field. However, performance issues and workload management issues due to the limitations of VM are reducing the resource utilization of HPC users. Therefore, we aim to provide a lightweight container-based cloud environment to HPC users. This container-based approach consists of two main components: the image management system and the workload management system. We have designed and implemented the system workflow and architecture considering ease of use and efficiency of management. The results have been obtained by comparing network performance, MPI performance and a simple machine learning code – MNIST between bare-metal and container-based (both in Docker and Singularity) environments.

(RP13) An Application Parameter Search Method Based on the Binary Search Algorithm for Performance Tuning

Takumi Kishitani (Tohoku University)

Because of the complexity of modern computer systems, such as many-core processors and heterogeneous memory systems, performance tuning is necessary to achieve high performance in scientific and engineering applications. The performance tuning needs to adjust many tuning parameters

provided by systems and applications. As the number of parameters increases, the number of their combinations to be searched increases. Moreover, the execution times of simulation applications become long because of their problem sizes and resolutions to solve. This situation causes an increase in a time for selecting an appropriate combination of the tuning parameters. This poster proposes the method to reduce the time to search the appropriate combination of the tuning parameters by the method based on the binary search algorithm. The proposed method select the appropriate application parameters such as inputs and iteration counts whiling keep the feature of the application. By executing the application with the smaller resolution and iteration counts than with original ones, each execution time for parameter tuning can be reduced. The evaluation results by using the tsunami simulation on Intel Xeon Phi Knights Landing show that the proposed method can select the most appropriate combination of the tuning parameters, and the parameter tuning time is reduced by 78.7% compared with the full search algorithm.

(RP14) Automatic Port to OpenACC/OpenMP for Climate & Weather Code Using the CLAW Compiler

Valentin Clement (ETH Zurich, Federal Office of Meteorology and Climatology MeteoSwiss)

In order to profit from emerging high-performance computing systems, weather and climate models need to be adapted to run efficiently on different hardware architectures such as accelerators. This is a major challenge for existing community models that represent very large code bases written in Fortran such as ICON. Large part of the code is ported using OpenACC compiler directives but for time-critical components such as physical parameterizations, code restructuring and optimizations are necessary to obtain optimal performance. In a effort to keep a single source code for multiple target architectures, the CLAW Compiler and the CLAW Single Column Abstraction (SCA) were introduced. In this poster, we extend the CLAW SCA to handle ELEMENTAL functions and subroutines to apply it to the JSBACH soil model of ICON. With this extension, the model can be automatically ported to OpenACC or OpenMP for accelerators with minimal to no change to the original code.

(RP15) Easy-to-use and Secure Web Command Line Interface for Heterogeneous Resources on Artificial Intelligence Platform

Rongqiang Cao (Computer Network Information Center, Chinese Academy of Sciences)

Command Line Interface (CLI) is still an important way to interact with computing resources today, but it is not easy for users to configure and access remote computing resources regarding network security and polices. Further, it is much difficult for users to learn many commands and adopt them to manage applications, tasks and data on different computing resources. We proposed event-based web services to smooth the sharp learning curve of CLI and will finally provide easy-to-use web CLI (WebCLI) services for users on our AI platform [http://ai.sccas.cn]. In WebCLI, command recommendation service is designed to help user write and complete a complicated command according to personal history commands, user's behaviors, the global data and different preference configurations. Command combination service is

designed to accept characters from a terminal running in browser and generate an entire command to shield syntax differences caused by various job management systems in heterogeneous resources. Security and risk service is designed to check whether each command gets permission to execute based on multi-levels white lists and black lists. It also present warnings to users if any command especially on delete will cause unrecoverable outcomes. Based on Eclipse Vert.x, a prototype was implemented to verify usability and availability. In a browser, a user can login CLI to access heterogeneous resources, query history commands in detail, and track each actions of a workflow. In future, we will continue to extend the prototype system to a productive system on the AI platform.

(RP16) Power Prediction with Probabilistic Topic Modeling for HPC

Shigeto Suzuki (FUJITSU LABORATORIES LTD.)

Hundreds-MW power will be required for exa-scale supercomputer in 2023, so the power consumption becomes a critical factor for the next-generation systems. A power-aware scheduling with job power prediction is a key technology to achieve energy-efficient operation and high system utilization. Recently, there is a significant number of researches about predicting job power from job entries such as user-id, number of nodes by using machine learning. One challenge for making these approaches into realization is tough tuning of weights for each job entries because the weights of each job entries is different for each site. In this work, we develop the novel two-step power prediction model combining topic model and probabilistic model. The model can predict each job power from submitted job entries without manual tuning of the weight. First, all the job entries of a target job are fed to the trained topic model to derive 10 candidate jobs from the past job database. Then, the probabilistic model selects one job from the 10 candidates that has the highest probability of success and uses its power as a prediction of the target job. The probabilistic model has automatically trained how to weight these job entries based on the relationship between the past entries and the power prediction results. We demonstrated 3-month power prediction of K computer. The average relative error with 18 % was achieved for the total job power prediction. The proposed two-step scheme has better accuracy of 3.1% in comparison with one-step, topic model only, scheme.

(RP17) Cross-Architecture Affinity of Supercomputers

Edgar A. Leon (Lawrence Livermore National Laboratory)

To reach exascale computing, vendors are developing complex systems that may include many-core technologies, hybrid machines with throughput-optimized cores and latency-optimized cores, and multiple levels of memory. The complexity involved in extracting the performance benefits these systems offer challenges the productivity of computational scientists greatly. A significant part of this challenge involves mapping parallel applications efficiently to the underlying hardware. A poor mapping may result in dramatic performance loss. Furthermore, an application mapping is often machine-dependent breaking portability to favor performance.

In this poster, I demonstrate that the memory hierarchy of a system is key to achieve performance-portable mappings of parallel applications. I leverage a memory-driven algorithm called mpibind that employs a simple interface computational scientists can use to map applications and results in a full mapping of MPI tasks, threads, and GPU kernels to hardware processing units and memory domains. The interface is simple and portable: a hybrid application and a number of tasks. This work applies the concept of memory-driven mappings to three emerging system architectures: a latency-optimized cores system, a two-level memory system, and a hybrid CPU+GPU system. Three use cases demonstrate the benefits of this approach: reducing system noise, improving application performance, and improving productivity. For example, an application developer can choose an advanced (and better performing) two-level memory configuration, use the same interface of a single-level memory, and still benefit from the performance advantages of the former.

(RP18) Real-Time Fire Detection Using CUDA

Manal Jalloul (American University of Beirut)

In this research, a high-resolution real-time fire detection system was implemented. NVIDIA CUDA framework was used to parallelize a serial version that was implemented using OpenCV. The algorithm relies on color thresholding with other de-noising image processing techniques applied to track the fire. Both implementations of the fire detection algorithm were compared, and the reported results show that the parallel implementation achieved a 60% speedup over the serial version.

(RP19) Scalable Network PDE-Based Multiphysics Simulation Using the PETSc Library

Hong Zhang (Argonne National Laboratory, Illinois Institute of Technology)

We present DMNetwork, a high-level set of routines included in the PETSc library for the simulation of multiphysical phenomena over large-scale networked systems. The library aims at applications that have networked structures such as the ones found in electrical, gas, and water distribution systems. DMNetwork provides data and topology management, parallelization for multiphysics systems over a network, and hierarchical and composable solvers to exploit the problem structure. DMNetwork eases the simulation development cycle by providing the necessary infrastructure through simple abstractions to define and query the network components.

We will demonstrates its ability to simulate the Mississippi river network, and to solve a system over large networks of water pipe distribution with more than 2 billion variables on extreme-scale computers using up to 30,000 processors.

(RP20) Development of Training Environment for Deep Learning With Medical Images on

Supercomputer System Based on Asynchronous Parallel Bayesian Optimization

Yukihiro Nomura (The University of Tokyo Hospital)

Recently, deep learning has been exploited in the field of medical image analysis. However, deep learning requires large amounts of computational power, and optimization of numerous hyper-parameters largely affects the performance of deep learning. If a framework for training deep learning with hyper-parameter optimization on a supercomputer system can be realized, it is expected to accelerate training of deep learning with medical images. In this study, we described our novel environment for training deep learning with medical images on the Reedbush-H supercomputer system based on asynchronous parallel Bayesian optimization (BO). Our training environment was composed of an automated hyper-parameter tuning module based on BO and a job submission module based on Xcrypt, which is a job level parallel script language based on Perl. The training jobs using the hyper-parameters generated by the hyper-parameter tuning module were alternately executed at the compute nodes. In training of deep learning using our framework, the hyper-parameters were chosen by BO so as to maximize the value of evaluation criteria in validation. We targeted an automated detection of lung nodule in chest computed tomography images based on a 3D U-Net. In this case, we selected 11 types of hyper-parameters. The tuning performance with sequential BO was superior to that with asynchronous parallel BO. When the number of workers was eight or less, the tuning performance with asynchronous parallel BO was superior to that with random search. The constructed environment enabled to efficiently train deep learning with hyper-parameter tuning on the Reedbush-H supercomputer system.

(RP21) Optimizing Deep Learning LSTM Topologies on Intel Xeon Architecture

Alexander Heinecke (Intel)

Long short-term memory (LSTM) is a type of recurrent neural network which is well-suited for processing temporal data. In this work, we present an optimized implementation of LSTM cell for Intel Xeon architecture. Typical implementations of the LSTM cell employ one or two large GEMM calls and then apply the element-wise operations (sigmoid/tanh) onto the GEMM results. While this approach is easy to implement by exploiting vendor-optimized GEMM library calls, the data reuse relies on how GEMMs are parallelized and is sub-optimal for GEMM sizes stemming from small minibatch. Also, the element-wise operations are exposed as a bandwidth-bound kernel after the GEMM which is typically a compute-bound kernel. To address this discrepancy, we implemented a parallel blocked matrix GEMM in order to (a) achieve load balance, (b) maximize weight matrix reuse, (c) fuse the element-wise operations after partial GEMM blocks are computed and while they are hot in cache. Additionally, we bring the time step loop in our cell to further increase the weight reuse and amortize the overhead to transform the weights into blocked layout. The results show that our forward pass can be up to 1.4x faster compared to MKL-DNN implementation, whereas the backward/update pass can be up to 1.3x faster. Furthermore, we modified TensorFlow framework to use our LSTM cell for end-to-end training of Google's neural machine translation application and attained identical BLEU score in as many iterations as original TensorFlow implementation while showcasing 1.9x speed up for 8-layer German-to-English translation model.

(RP22) Supercomputer-Scale Training of Large AI Radiology Models

Valeriu Codreanu (SURFsara)

The health care industry is expected to be an early adopter of AI and deep learning to improve patient outcomes, reduce costs, and speed up diagnosis. We have developed models for using AI to diagnose pneumonia, emphysema, and other thoracic pathologies from chest x-rays. Using the Stanford University CheXNet model as inspiration, we explore ways of developing highly-accurate models for this problem with fast parallel training on Zenith, the Intel Xeon-based supercomputer at Dell EMC's HPC and AI Innovation Lab. We explore various network topologies to gain insight into what types of neural networks scale well and improve training time from days to hours, while at the same time giving significantly better predictions . We then explore transferring this learned knowledge to other radiology subdomains, such as mammography, and whether this leads to better models than developing subdomain models independently.

(RP23) A Skewed Multi-Bank Cache for Vector Processors

Hikaru Takayashiki (Tohoku University)

Vector supercomputers are widely used in scientific and engineering applications that require a high memory bandwidth. Recently, the key component of the vector supercomputers, a vector processor, has adopted a multi-core architecture that plays an important role for improving computing performance. On the other hand, improvement of the memory bandwidth is limited due to memory technology trends. Hence, the vector processor employs multi-bank cache memories in order to obtain high memory data transfer capability. It is expected that these trends continue, and more cores and caches with more banks will be used even in future vector processors. However, cache configurations suitable for vector processors are not clear in the case of many cores and many cache banks. The preliminary evaluation using a simulator shows that a vector processor with many cores and many banks causes a lot of conflict misses in the stencil kernel. Therefore, this poster proposes a skewed multi-bank cache for the many-core vector processors that enables to suppress conflict misses with a low associativity. This poster examines odd-multiplier displacement hashing as a hash function for skewing and SRRIP as a cache replacement policy. The evaluation results show that, by adopting the skewed multi-bank cache for a many-core vector processor, almost ideal hit ratio can be obtained in the stencil kernel.

(RP25) Development of Performance Assessment Method Based on Aspen DSL and Micro-Kernels Benchmarking

Ekaterina Tyutlyaeva (RSC Technologies)

Accurate assessment and predicting the applications performance are essential for the effective usage of

modern multi-core computers. Performance models can allow to describe the dynamical behavior of applications on different computing platforms so they can be useful for the design of future supercomputers. In this research, we propose the application performance assessment method based on Aspen DSL modeling complimented with direct performance measurements and experimental data analyzing. On the poster an analytical performance model for multispectral images processing application is presented as an example of more general approach. The model construction steps include application profiling, experimental direct measurements of actual FLOPs, processor cycles and different memory usage data.

(RP27) Memory First : A Performance Tuning Strategy Focusing on Memory Access Patterns
Naoki Ebata (Tohoku University)

As many scientific applications are memory-bound, a key to achieving high sustained performance on a modern HPC system is to fully exploit the system's memory bandwidth. Indeed, the sustained memory bandwidth of an application could be much lower than the theoretical peak bandwidth of the system for various reasons due to underlying memory architectures. For example, a certain memory access pattern may cause frequent access conflicts at memory channels and/or banks, and thus lead to a longer access latency. This poster hence discusses a memory-centric performance tuning strategy, Memory First. Usually, a whole application is first written and then optimized for a particular system, often resulting in major code modifications for memory-aware tuning. On the other hand, in the Memory First strategy, memory access patterns capable of achieving high sustained memory bandwidths on a target system are first investigated. Then, unlike the conventional strategy, a tiny benchmark code achieving a high sustained memory bandwidth is developed, while keeping a target application's behavior in mind. Finally, the code is modified to work as the target application. While application coding is well established in matured application areas such as CFD, memory-aware tuning is likely to become more painful in practice. This is because the latter has to be developed for every new architecture in a try-and-error fashion. Therefore, giving a higher priority to memory-aware tuning can result in a lower tuning cost in modern HPC systems with advanced memory technologies, such as NEC SX-Aurora TSUBASA.

(RP28) Performance Tuning of Deep Learning Framework Chainer on the K Computer.
Akiyoshi Kuroda (RIKEN, R-CCS)

Recently the applications and research of machine learning by deep learning has become popular using GPU. However, it seems possible to do many calculations using CPUs of massively parallel computers. Here, we introduce some performance tuning procedures for Chainer, which is a representative framework for utilization of machine learning on the K computer. Chainer expresses the hierarchical structure of deep learning using Python, and all calculations can be realized using numPy without special libraries. By optimizing floating point underflow exception when building Python, elapsed time was improved to 1/3.39. Moreover, by replacing the SSL2 gemm library called by Python with the thread-

parallel version, section elapsed time was improved to 1/4.54, the total elapsed time was improved to 1/1.15, and the performance efficiency was improved about 47.0%. Many of the cost was the calculation of the square root and the arithmetic when the filter was updated and activation functions. These operations are not optimized when calculated using numPy and are particularly slow on the K computer. By replacing the kernel with software pipelining and SIMD optimization by Fortran library, the kernel elapsed time was improved to 1/11.08 and total elapsed time was improved to 1/16.23. There are some limitations on the use of Chainer on the K computer. However, it can be said that deep learning calculation became possible on the K computer and the Post-K computer using these tuning effect and CPU parallel version Chainer.

Closing & Transition to the Poster Reception
Sunita Chandrasekaran (University of Delaware), Ryusuke Egawa (Tohoku University)

Room: Areal
10:00 am - 11:00 am

Reception & ISC Research Poster Awards

Room: Areal
11:00 am - 4:45 pm

Research Posters + PhD Forum Posters + HPC in Asia Posters

Session Description: For a complete list of the Research Posters on display at ISC 2019, please refer to the
overview
of the Research Posters Session on Tuesday, June 18. For a complete list of the PhD Forum Posters on display at ISC 2019, please refer to the
overview
of the PhD Forum Posters Session on Monday, June 17. For a complete list of the HPC in Asia Posters on display at ISC 2019, please refer to the
overview
of the HPC in Asia Posters Session on Wednesday, June 19. For a complete list of the Woman in HPC Posters on display at ISC 2019, please refer to the
overview

of the Woman in HPC Posters on Tuesday, June 18.

Wednesday, June 19th

Room: Areal
8:30 am - 5:00 pm

Research Posters + PhD Forum Posters + HPC in Asia Posters

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Social Event

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Sunday, June 16th

Room: Areal
6:00 pm - 8:30 pm

Pre-Conference Party

Session Description: Arriving on Saturday or Sunday for ISC 2019? Plan to join our Pre-Conference Party! This Sunday evening party allows ISC attendees and exhibitors alike the possibility to catch up with new and familiar faces in a casual setting and ahead of a busy week. To help you ignore the jetlag, we have packed the evening with various entertainment activities:
Science slam
, popular music, and of course food and drinks. Come join the fun! The party is open to all, but is limited to the first 400 attendees.

Monday, June 17th

Room: Exhibition Hall
6:30 pm - 8:30 pm

Exhibition Party

Session Description: The ISC Exhibition Party is a traditional welcome to the ISC showfloor, allowing you to meet over 160 industry and research exhibitors face-to-face. This evening event sets a tone for the entire ISC Exhibition. Food and drinks will be served with ambient lounge music playing in the background, and thus putting you in the right mood to shop for HPC solutions. Also look out for our graphic recorder, Ms. Hübner, who'll be there to capture the Monday ISC Exhibition in the form of graphic art.

Special Event

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Monday, June 17th

Room: Konstant
1:00 pm - 2:00 pm

ISC First-Time Attendee Session

Session Description: The ISC First-Time Attendee Session is intended as an introductory session for ISC High Performance attendees who want to learn to navigate through the 2019 conference, make the best use of their time at the event, and have fun meeting other HPC practitioners. Besides helping you navigate, we would also like to introduce you to the inclusivity efforts at ISC 2019. As a conference we strive to make everyone feel welcome and comfortable. Please also join this session for a get together with other first-time attendees.

First Time Attendee Session
Kimberly McMahon (McMahon Consulting), Laura Schulz (Leibniz Supercomputing Centre)

First time here? Come join us for an overview of all the happenings of ISC19 and learn how to make the most of your week. Meet fellow attendees and pick up tips on best things to see and do. Learn about our inclusivity efforts to build and bridge the HPC village.

Join us for a fun, informative hour and leave with new knowledge and community friends.

Room: Panorama 2
6:00 pm - 6:45 pm

Intel HPC Special

Intel's Architectural Vision for HPC
Rajeeb Hazra (Intel)

Join Dr. Rajeeb Hazra, Corporate VP and GM, Enterprise & Government Group at Intel, for a presentation on Monday, June 17th 2019 at 6:00pm. Dr. Hazra will discuss Intel's investments to drive the convergence of HPC and AI and highlight how innovations across the platform will pave the path to Exascale to address the world's toughest challenges. Visit us in booth #F-930.

Tuesday, June 18th

Room: Panorama 2
12:30 pm - 1:00 pm

HPC in Germany - An Update from GCS

HPC in Germany - An Update from GCS
Dieter Kranzlmüller (Leibniz Supercomputing Centre (LRZ))

The Gauss Center for Supercomputing (GCS) has just procured its next generation of HPC systems for Germany. Each system at the three national supercomputing centers in Garching, Jülich and Stuttgart offers more than 10 PetaFlop/s (10^16 Flop/s) of performance. This update from GC, showcases the latest installations and their capabilities and introduces an outlook on the future developments towards exascale. At the core of the GCS strategy is the increasing demand from the user communities, which drive the planning by requesting higher computational performance, better scalability, and improved throughput for the benefits of science and research. This user-driven approach underlines the goals of the German Smart Scaling Initiative to establish a powerful German HPC ecosystem, complementing European and international initiatives.

Student Cluster Competition

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Wednesday, June 19th

Room: Panorama 2
5:15 pm - 5:30 pm

HPCAC-ISC Student Cluster Competition 2019 Award Ceremony

Student Program

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Wednesday, June 19th

Room: Kontrast
9:30 am - 11:00 am

ISC STEM Student Day 01

Session Description: The ISC STEM Student Day & Gala welcomes science, technology, engineering, and mathematics (STEM) students into the world of high performance computing, and demonstrate the opportunities this industry offers young talents, in terms of training and future careers. Attendees will receive a systematic introduction to the technology and industry key players, starting with a morning tutorial and ending with a career fair. The ISC STEM Student Day & Gala sign up opens April 09 and will officially close when the program reaches 200 participants. Contact communications@isc-group.com for further information.

HPC Tutorial: Applications, Systems, and Programming Models (two parts)
Bernd Mohr (Jülich Supercomputing Centre)

High Performance Computing (HPC) is a fundamental technology used in solving scientific and commercial problems. Many of the grand challenges of science depend on simulations and models run on HPC facilities to make progress, for example: protein folding, understanding the human brain, or developing nuclear fusion. In industry, sophisticated computer models are integral to the development of products such as jet engines, wind turbines and new drugs.

In this introductory tutorial, you will learn what "high performance computing" means and what differentiates it from more mainstream areas of computing. You will also be introduced to the major applications that use high performance computing for research and commercial purposes, as well as the systems needed to run these applications. Finally, you will be provided with an overview of the languages and paradigms used to program HPC applications and systems.

Room: Kontrast
11:30 am - 12:30 pm

ISC STEM Student Day 02

Session Description: The ISC STEM Student Day & Gala welcomes science, technology, engineering, and mathematics (STEM) students into the world of high performance computing, and demonstrate the opportunities this industry offers young talents, in terms of training and future careers. Attendees will receive a systematic introduction to the technology and industry key players, starting with a morning tutorial and ending with a career fair. The ISC STEM Student Day & Gala sign up opens April 09 and will officially close when the program reaches 200 participants. Contact communications@isc-group.com for further information.

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Room:
6:45 pm - 9:30 pm

ISC STEM Student Gala

Session Description: The ISC STEM Student Day & Gala welcomes science, technology, engineering, and mathematics (STEM) students into the world of high performance computing, and demonstrate the opportunities this industry offers young talents, in terms of training and future careers. Attendees will receive a systematic introduction to the technology and industry key players, starting with a morning tutorial and ending with a career fair. The ISC STEM Student Day & Gala sign up opens April 09 and will

officially close when the program reaches 200 participants. Contact communications@isc-group.com for further information.

Welcome and Drinks

Big Hair, Big Data And Beyond - A Career Perspective In Enterprise Computing
Arno Kolster (Providentia Worldwide)

As part of STEM day, Mr. Kolster shares stories and insights into his computer career in industry and the advent of HPC integration in commercial environments. A 30 year long career in various industries including oil and gas, energy and e-commerce provides a unique perspective on how HPC is impacting industry, now and in the future. This discussion will provide insights for developing a career path to take advantage of the multi-faceted growth of HPC in the enterprise. It will also showcase the rapid technological changes that have happened and the impact to industry, business and the general public.

For the attendees that are just embarking on their careers, this will be a good introduction to the career possibilities that exist.

There will be also be many anecdotes, personal experiences and hopefully a few laughs.

Dinner, Networking & Career Fair

Tutorial

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Sunday, June 16th

Room: Analog 1
9:00 am - 1:00 pm

OpenMP Common Core: Learning Parallelization of Real Applications from the Ground-Up

OpenMP Common Core: Learning Parallelization of Real Applications from the Ground-Up
Manuel Arenaz (University of A Coruña, Appentra Solutions), Barbara Chapman (Stony Brook University), Oscar Hernandez (Oak Ridge National Laboratories), Javier Novo Rodriguez (Appentra Solutions)

As HPC continues to move towards a model of multicore and accelerator programming, a detailed understanding of shared-memory models and how best to use accelerators has never been more important. OpenMP is the de facto standard for writing multithreaded code to take advantage of shared memory platforms, but to make optimal use of it can be incredibly complex.

With a specification running to over 500 pages, OpenMP has grown into an intimidating API viewed by many as for “experts only”. This tutorial will focus on the 16 most widely used constructs that make up the ‘OpenMP common core’. We will present a unique, productivity-oriented approach by introducing its usage based on common motifs in scientific code, and how each one will be parallelized. This will enable attendees to focus on the parallelization of components and how components combine in real applications.

Attendees will use active learning through a carefully selected set of exercises, building knowledge on parallelization of key motifs (e.g. matrix multiplication, map reduce) that are valid across multiple scientific codes in everything from CFD to Molecular Simulation.

Attendees will need to bring their own laptop with an OpenMP compiler installed (more information at www.openmp.org).

Room: Kolleg
9:00 am - 1:00 pm

Managing HPC Software Complexity with Spack

Managing HPC Software Complexity with Spack
Todd Gamblin (LLNL), Gregory Becker (LLNL), Massimiliano Culpo (EPFL), Michael Kuhn (Universität Hamburg), Peter Scheibel (LLNL)

The modern scientific software stack includes thousands of packages, from C, C++, and Fortran libraries, to packages written in interpreted languages like Python and R. HPC applications may depend on hundreds of packages spanning all of these ecosystems. To achieve high performance, they must also leverage low-level and difficult-to-build libraries such as MPI, BLAS, and LAPACK. Integrating this stack is extremely challenging. The complexity can be an obstacle to deployment at HPC sites and deters developers from building on each others' work.

Spack is an open source tool for HPC package management that simplifies building, installing, customizing, and sharing HPC software stacks. In the past few years, its adoption has grown rapidly: by end-users, by HPC developers, and by the world's largest HPC centers. Spack provides a powerful and flexible dependency model, a simple Python syntax for writing package build recipes, and a repository of over 3,200 community-maintained packages. This half-day tutorial provides an introduction to Spack's capabilities: basic usage, installing and authoring packages, and previews of more advanced features such as module generation and virtual environments. Attendees will leave with skills for using Spack to automate day-to-day tasks, along with the foundation they need to take on more advanced use cases.

Room: Konstant
9:00 am - 1:00 pm

InfiniBand, Omni-Path, and High-speed Ethernet for Beginners

InfiniBand, Omni-Path, and High-speed Ethernet for Beginners
Dhabaleswar Panda (The Ohio State University), Hari Subramoni (The Ohio State University)

InfiniBand (IB), Omni-Path, and High-speed Ethernet (HSE) technologies are generating a lot of excitement towards building next generation High-End Computing (HEC) systems including clusters, datacenters, file systems, storage, cloud computing and Big Data (Hadoop, Spark, HBase and Memcached) environments. RDMA over Converged Enhanced Ethernet (RoCE) technology is also getting widely deployed. This tutorial will provide an overview of these emerging technologies, their

offered architectural features, their current market standing, and their suitability for designing HEC systems. It will start with a brief overview of IB, Omni-Path, and HSE. In-depth overview of the architectural features of IB, Omni-Path, and HSE (including iWARP and RoCE), their similarities and differences, and the associated protocols will be presented. Next, an overview of the OpenFabrics stack which encapsulates IB, HSE, and RoCE (v1/v2) in a unified manner will be presented. An overview of libfabrics stack will also be provided. Hardware/software solutions and the market trends behind IB, Omni-Path, HSE, and RoCE will be highlighted. Finally, sample performance numbers of these technologies and protocols for different environments will be presented.

Room: Effekt
9:00 am - 1:00 pm

Hands-on Practical Hybrid Parallel Application Performance Engineering

Hands-on Practical Hybrid Parallel Application Performance Engineering
Christian Feld (Jülich Supercomputing Center), Markus Geimer (Jülich Supercomputing Center), Sameer Shende (University of Oregon; ParaTools, Inc.), Bill Williams (Technische Universität Dresden)

This tutorial presents state-of-the-art performance tools for leading-edge HPC systems founded on the community-developed Score-P instrumentation and measurement infrastructure, demonstrating how they can be used for performance engineering of effective scientific applications based on standard MPI, OpenMP, hybrid combination of both, and increasingly common usage of accelerators. Parallel performance tools from the Virtual Institute – High Productivity Supercomputing (VI-HPS) are introduced and featured in hands-on exercises with Cube, Vampir, and TAU. We present the complete workflow of performance engineering, including instrumentation, measurement (profiling and tracing, timing and PAPI hardware counters), data storage, analysis, tuning, and visualization. While measurement collection using Score-P and automatic trace analysis with Scalasca will be demonstrated, emphasis is placed on analyzing measurement results and how tools are used in combination for identifying performance problems and investigating optimization alternatives. Using their own notebook computers with a provided HPC Linux [http://www.hpclinux.org] OVA image containing all of the necessary tools (running within a virtual machine), participants will conduct hands-on exercises on prepared example measurements from Score-P and Scalasca collected on contemporary HPC systems. This will help to prepare participants to locate and diagnose performance bottlenecks in their own parallel programs.

Room: Expose
9:00 am - 1:00 pm

Arm's Scalable Vector Extension: Programming Tools and Performance Analysis

Arm's Scalable Vector Extension: Programming Tools and Performance Analysis
John Linford (Arm), Oliver Perks (Arm), Daniel Ruiz Munoz (Arm)

The Scalable Vector Extension (SVE) is the next-generation SIMD instruction set for Armv8-A. SVE does not specify a vector length and it uses predicates to dynamically select the vector lanes on which an instruction operates. For many application developers, this presents an entirely new way of thinking about vectorization. This tutorial will introduce tools for SVE programming and performance analysis, and through hands-on exercises will explore the unique features of SVE and demonstrate their applicability to a range of common programing motifs. The tutorial will demonstrate how to capture high-utility information and present it in meaningful ways, such as how much time is spent in application routines, where these routines are called in the source code, and how well the routines vectorize. Programmers will be introduced to the Arm C Language Extensions, which provides a set of types and accessors for SVE vectors and predicates and a function interface for all relevant SVE instructions. This tutorial will also demonstrate how the Arm Instruction Emulator may be used to execute SVE codes and gage the quality of SVE vectorization. Attendees will complete the tutorial with a working understanding of SVE and knowledge of how SVE may be used in their applications.

Room: Extrakt
9:00 am - 1:00 pm

Boosting Power Efficiency of HPC Applications with GEOPM

Boosting Power Efficiency of HPC Applications with GEOPM
Martin Schulz (Technical University of Munich, Leibniz Supercomputing Centre (LRZ)), Aniruddha Marathe (Lawrence Livermore National Laboratory), Jonathan Eastep (Intel Corporation), Matthias Maiterth (Ludwig Maximilian University Munich (LMU), Intel Corporation), Siddhartha Jana (Energy Efficient HPC Working Group), Todd Rosedahl (IBM), Torsten Wilde (HPE), Stephanie Brink (Lawrence Livermore National Laboratory)

Power and energy are critical Exascale constraints. Achieving system efficiency is a challenge under such constraints due to dynamic application phase behavior, increasing variation in processor power efficiency resulting from manufacturing, and due to complexities arising from upcoming heterogeneous architectures. In order to address some of these challenges, Intel introduced GEOPM, an open-source, portable, hierarchical job-level runtime system to optimize for time-to-solution by leveraging techniques from learning and control systems. Other processor architectures like IBM POWER and ARM have recognized the value of GEOPM, and are currently working to add their specific processor support. In this

hands-on, half-day tutorial, we will discuss the state-of-the-art power management techniques used by Intel, IBM, and ARM, and discuss GEOPM features and usability. A high-level overview of the GEOPM architecture, a walkthrough of the GEOPM plugin infrastructure, and use cases will be discussed. Third-party plugins developed as part of Exascale Computing Project's GEOPM plugins will also be demoed. Algorithms used to speed up application critical path (through adaptive configuration selection) and mitigate process variation (through intelligent power management) will be discussed. State-of-the-art and best practices for leveraging power management techniques in modern processors will also be covered.

Room: Monte Rosa 1,2
9:00 am - 1:00 pm

HPC Strategy, Procurement, Cost Models and Metrics

HPC Strategy, Procurement, Cost Models and Metrics
Andrew Jones (Numerical Algorithms Group (NAG)), Ingrid Barcena (KU Leuven), Michael Croucher (Numerical Algorithms Group (NAG))

HPC leadership and management skills are essential to the success of HPC. This includes securing funding, procuring the right technology, building effective support teams, ensuring value for money, and delivering a high-quality service to users. However, whilst programmers, sysadmins and users are well-catered for with tutorials at ISC, good quality training for HPC leaders and managers has been notably missing.

This tutorial will provide practical experience-based training on core business aspects of HPC, including strategy, delivery options, hardware procurement, total cost of ownership, metrics and value.

The lead author has become the de-facto international leader in delivering training on these topics, with a desire to improve the best practice of the community, and without a sales focus or product to favour. The HPC leadership tutorials by these authors have been strongly attended and highly rated by attendees at SC for several years, and have been successful in several other formats and venues.

Room: Matterhorn 1
9:00 am - 1:00 pm

Compression for Scientific Data

Compression for Scientific Data

franck cappello (Argonne National Laboratory), Peter Lindstrom (Lawrence Livermore National Laboratory)

Large-scale numerical simulations, observations and experiments are generating very large datasets that are difficult to analyze, store and transfer. Data compression is an attractive and efficient technique to significantly reduce the size of scientific datasets. This tutorial reviews the state of the art in lossy compression of scientific datasets, discusses in detail two lossy compressors (SZ and ZFP), introduces compression error assessment metrics and the Z-checker tool to analyze the difference between initial and decompressed datasets. The tutorial will offer hands-on exercises using SZ and ZFP as well as Z-checker. The tutorial addresses the following questions: Why lossless and lossy compression? How does compression work? How measure and control compression error? The tutorial uses examples of real-world compressors and scientific datasets to illustrate the different compression techniques and their performance. Participants will also have the opportunity to learn how to use SZ, ZFP and Z-checker for their own datasets. The tutorial is given by two of the leading teams in this domain and targets primarily beginners interested in learning about lossy compression for scientific data. This half-day tutorial is improved from the evaluations of the highly rated tutorials given on this topic at ISC17, SC17 and SC18.

Room: Analog 2
9:00 am - 6:00 pm

GPU Bootcamp - A Collaborative Hands-on GPU Tutorial

GPU Bootcamp - A Collaborative Hands-on GPU Tutorial

Michael Wolfe (NVIDIA), Andreas Herten (Jülich Supercomputing Centre)

GPU bootcamp is a collaborative hands-on tutorial designed to teach scientists and researchers how to start quickly accelerating codes on GPUs. Participants will be given an overview of available GPU libraries, programming models, and platforms, followed by a deep dive on the basics of GPU programming using OpenACC through extensive hands-on collaboration based on real-life codes. OpenACC lectures and labs will be paired together with a working session where participants will work in teams to accelerate one or several mini-applications on GPUs.

OpenACC is a centerpiece of this tutorial as it is a proven programming model chosen by top HPC applications. The model helps scientists and researchers start programming GPUs with significantly less effort than is required with a low-level model such as OpenCL or CUDA. OpenACC is used together with GPU-accelerated libraries to simplify the first steps of running their code on GPUs so participants can get

results faster and understand GPU programming. Applications ported to GPUs using OpenACC can also run in parallel on all the cores of a multi-core CPU without any code modification by simply recompiling for the different targets. This enables development on CPU-only systems if or when GPUs are not available.

Room: Applaus
9:00 am - 6:00 pm

Advanced MPI

Advanced MPI

Pavan Balaji (Argonne National Laboratory), Torsten Hoefler (ETH Zurich), Antonio J. Peña (Barcelona Supercomputing Center), Yanfei Guo (Argonne National Laboratory)

The Message Passing Interface (MPI) has been the de facto standard for parallel programming for nearly two decades now. However, a vast majority of applications only rely on basic MPI-1 features without taking advantage of the rich set of functionality the rest of the standard provides. Further, with the advent of MPI-3 (released in September 2012), a vast number of new features have been introduced in MPI, including efficient one-sided communication, support for external tools, non-blocking collective operations, and improved support for topology-aware data movement. The upcoming MPI-4 standard aims at introducing further improvements to the standard in a number of aspects. This is an advanced-level tutorial that will provide an overview of various powerful features in MPI, especially with MPI-2 and MPI-3, and will present a brief preview into what is being planned for MPI-4.

Room: Substanz 1, 2
9:00 am - 6:00 pm

Quantum Computing for Scientific Applications in the Noisy Intermediate-Scale Quantum Device Era

Quantum Computing for Scientific Applications in the Noisy Intermediate-Scale Quantum Device Era

Costin Iancu (LBNL), Wibe de Jong (LBNL), Ojas Parekh (Sandia National Laboratories), Tzvetan Metodi (Sandia National Laboratories), Eugene Dumitrescu (Oak Ridge National Laboratory), Sarah Powers (Oak Ridge National Laboratory)

Quantum computing is an emerging technology that promises to revolutionize many computational tasks. However, for a non-specialist it may appear that it is surrounded by a shroud of hype and misconception. The main goal of this tutorial is to demystify practical quantum computing and all its vital algorithmic aspects to a general audience of computer scientists with little to no prior knowledge of the subject. We plan to achieve this through a combination of lecture materials, demonstrations and hands on exercises delivered by quantum computing experts with extensive experience in public speaking and teaching from the US Department of Energy Research Laboratories (DOE) and academia. In particular, we aim to elucidate quantum computing use for scientific applications, covering the following areas: 1) quantum algorithm design; 2) quantum programming toolkits; 3) practical error mitigation for quantum algorithms. We will focus on the design and implementation of hybrid quantum-classical computational strategies including variational quantum eigensolver (VQE) and quantum approximate optimization algorithms (QAOA) in the context of quantum chemistry, nuclear structure, graph partitioning, telecommunication networks and quantum field theory problems. We will discuss multiple practical ways to mitigate systematic coherent errors in the nascent quantum hardware, including general techniques such as randomized compilation.

Room: Matterhorn 2
9:00 am - 6:00 pm

Deep Learning at Scale

Deep Learning at Scale
Thorsten Kurth (Lawrence Berkeley National Laboratory), Steven Farrell (Lawrence Berkeley National Laboratory), Mustafa Mustafa (Lawrence Berkeley National Laboratory), Mike Ringenburg (Cray)

Deep learning is rapidly and fundamentally transforming the way science and industry use data to solve challenging problems. Deep neural network models have been shown to be powerful tools for extracting insights from data across a large number of domains. As these models grow in complexity to solve increasingly challenging problems with larger and larger datasets, the need for scalable methods and software to train them grows accordingly.

This tutorial will continue and expand upon our well attended tutorial at Supercomputing 18 and aims to provide attendees with a working knowledge on deep learning on HPC class systems, including core concepts, scientific applications, and techniques for scaling. We will provide training accounts and example Jupyter notebook-based exercises, as well as datasets, to allow attendees to experiment hands-on with training, inference, and scaling of deep neural network machine learning models.

Room: Analog 1
2:00 pm - 6:00 pm

Advanced OpenMP: Performance and 5.0 Features

Advanced OpenMP: Performance and 5.0 Features
Christian Terboven (RWTH Aachen University), Michael Klemm (Intel), Kelvin Li (IBM), Bronis R. de Supinski (Lawrence Livermore National Laboratory)

With the increasing prevalence of multicore processors, shared-memory programming models are essential. OpenMP is a popular, portable, widely supported and easy-to-use shared-memory model. Developers usually find OpenMP easy to learn. However, they are often disappointed with the performance and scalability of the resulting code. This disappointment stems not from shortcomings of OpenMP but rather from the lack of depth with which it is employed. Our “Advanced OpenMP Programming” tutorial addresses this critical need by exploring the implications of possible OpenMP parallelization strategies, both in terms of correctness and performance.

While we quickly review the basics of OpenMP programming, we assume attendees understand basic parallelization concepts and will easily grasp those basics. In two parts we discuss language features in-depth, with emphasis on advanced features like vectorization and compute acceleration. In the first part, we focus on performance aspects, such as data and thread locality on NUMA architectures, and exploitation of the comparably new language features. The second part is a presentation of the directives for attached compute accelerators.

Room: Kolleg
2:00 pm - 6:00 pm

A Tour of LLVM, a Modern and Open Source HPC Compiler Framework

A Tour of LLVM, a Modern and Open Source HPC Compiler Framework
Simon Moll (Saarland University), Johannes Doerfert (Argonne National Laboratory), Joel Denny (Oak Ridge National Laboratory), Sameer Shende (University of Oregon)

LLVM, a modern, industry-backed, open source compiler framework is well-known in the compiler research community, as a back-end for emerging program languages, and for software tooling tasks. While efforts like the exascale initiative, lead by various research facilities and HPC companies, are continuously improving the LLVM codebase and language front-ends, e.g., Clang and Flang, to support

HPC workloads, LLVM is still underutilized in the HPC community. This tutorial we will augment the development efforts through community outreach and hands-on interactions for novice and experienced users interested in topics like OpenMP, OpenACC, modeling, Vectorization, and Performance Analysis.

In this tutorial, we will introduce the LLVM framework, including the front-ends that support HPC-related languages, e.g. OpenMP, OpenACC, and Fortran. We will discuss HPC related optimization capabilities with a focus on vectorized and parallelized programs. Additionally, we show how the LLVM framework in combination with the TAU Performance System allows accurate performance analysis of parallel HPC applications. Each tutorial part will allow for hands-on participation and encourage questions from the audience.

Room: Konstant
2:00 pm - 6:00 pm

Better Scientific Software

Better Scientific Software
David E. Bernholdt (Oak Ridge National Laboratory), Anshu Dubey (Argonne National Laboratory), Jared O'Neal (Argonne National Laboratory)

The computational science and engineering (CSE) community is in the midst of an extremely challenging period created by the confluence of disruptive changes in computing architectures, demand for greater scientific reproducibility, and new opportunities for greatly improved simulation capabilities, especially through coupling physics and scales. Computer architecture changes require new software design and implementation strategies, including significant refactoring of existing code. Reproducibility demands require more rigor across the entire software endeavor. Code coupling requires aggregate team interactions including integration of software processes and practices. These challenges demand large investments in scientific software development and improved practices. Focusing on improved developer productivity and software sustainability is both urgent and essential.

This tutorial will provide information about software practices, processes, and tools explicitly tailored for CSE. Goals are improving the productivity of those who develop CSE software and increasing the sustainability of software artifacts. We discuss practices that are relevant for projects of all sizes, with emphasis on small teams, and on aggregate teams composed of small teams. Topics include effective models, tools, and processes for small teams (including agile workflow management), reproducibility, and scientific software testing (including automated testing and continuous integration).

Room: Effekt
2:00 pm - 6:00 pm

High Performance Distributed Deep Learning: A Beginner's Guide

High Performance Distributed Deep Learning: A Beginner's Guide
Dhabaleswar Panda (The Ohio State University), Ammar Ahmad Awan (The Ohio State University), Hari Subramoni (The Ohio State University)

The current wave of advances in Deep Learning (DL) has led to many exciting challenges and opportunities for Computer Science and Artificial Intelligence researchers alike. DL frameworks like TensorFlow, PyTorch, Caffe, and several others have emerged that offer ease of use and flexibility to describe, train, and deploy various types of Deep Neural Networks (DNNs). In this tutorial, we will provide an overview of interesting trends in DNN design and how cutting-edge hardware architectures are playing a key role in moving the field forward. We will also present an overview of different DNN architectures and DL frameworks. Most DL frameworks started with a single-node/single-GPU design. However, approaches to parallelize the process of DNN training are also being actively explored. The DL community has moved along different distributed training designs that exploit communication runtimes like gRPC, MPI, and NCCL. In this context, we highlight new challenges and opportunities for communication runtimes to efficiently support distributed DNN training. We also highlight some of our co-design efforts to utilize CUDA-Aware MPI for large-scale DNN training on modern GPU clusters. Finally, we also include hands-on exercises to enable the attendees gain first-hand experience of running distributed DNN training experiments on a modern GPU cluster.

Room: Expose
2:00 pm - 6:00 pm

Performance Optimization of Scientific Codes with the Roofline Model

Performance Optimization of Scientific Codes with the Roofline Model
Charlene Yang (NERSC, LBNL), Zakhar Matveev (Intel), Aleksandar Ilic (Universidade de Lisboa), Diogo Marques (Universidade de Lisboa)

The Roofline performance model offers an insightful and intuitive way to identify performance bottlenecks and guide optimization efforts, and it has been increasingly popular in the HPC community. This tutorial will strengthen the community’s Roofline knowledge and empower the community with a more automated and systematic methodology for Roofline-based analysis on both CPU and GPU architectures. It will start

with an overview of the Roofline concepts and then focus on NVIDIA GPUs and present a practical methodology for Roofline data collection. With some examples, it will discuss how various characteristics such as arithmetic intensity, memory access pattern and thread divergence can be captured by the Roofline formularism on GPUs. The tutorial will then shift its focus to Intel CPUs and proceed with a hands-on, where Intel Advisor and its Roofline feature are introduced and a stencil code is used to demonstrate how Roofline can be used to guide optimization on Haswell and KNL architectures. The tutorial will conclude with a set of case studies illustrating effective usage of Roofline in real-life applications. Overall, this tutorial is a unique and novel combination of a solid methodology basis, highly practice-oriented demos and hands-on, and a representative set of open-science optimization use cases.

Room: Extrakt
2:00 pm - 6:00 pm

In situ Data Analysis and Visualization with SENSEI

In situ Data Analysis and Visualization with SENSEI
E. Wes Bethel (LBNL), Silvio Rizzi (Argonne National Lab), Burlen Loring (LBNL)

This tutorial presents the fundamentals of in situ data analysis and visualization leveraging the SENSEI generic in situ interface. We demonstrate the infrastructure to couple simulation codes to multiple tools: ParaView, VisIt, and custom Python-based methods. Attendees will learn the basics of in situ analysis and visualization, and will gain hands on experience instrumenting simple mini apps and real simulation codes. The SENSEI in situ framework gives simulations access to a diverse set of back end data consumers, such as ADIOS, Libsim, Catalyst, VTK-m, and Python, through a single data model and API. With SENSEI, the simulation selects the back-end at runtime through an XML configuration file allowing easy interchange of analysis tools. This tutorial is timely, because a key trend facing extreme-scale computational science is the widening gap between computational and I/O rates. The challenge is how to gain insight from simulation data best when it is increasingly impractical to save it to persistent storage for subsequent visualization and analysis. One approach to this challenge is the idea of in situ processing, where one performs visualization and analysis processing while data is still resident in memory.

Room: Monte Rosa 1,2
2:00 pm - 6:00 pm

Getting Started with Containers on HPC

Getting Started with Containers on HPC

Carlos Eduardo Arango (Sylabs), Andrew J. Younge (Sandia national Laboratories), Shane Canon (Lawrence Berkeley National Laboratory), Sameer Shende (University of Oregon)

Within just the past few years, the use of containers has revolutionized the way in which industries and enterprises have developed and deployed computational software and distributed systems. The containerization model is gaining traction within the HPC community as well with the promise of improved reliability, reproducibility, and levels customization that are not otherwise possible on supercomputers previously. From the onset of containerization in HPC, Singularity has lead the way in providing container services, ranging from small clusters to entire supercomputers.

This hands-on tutorial looks to train users on the usability of containers on HPC resources. Specifically, the tutorial will walk through the processes of creating, deploying, and running Singularity containers on a Linux cluster. We will provide a detailed background on Linux containers, along with introductory hands-on experience building and running containers on a cluster. Furthermore, the tutorial will provide more advanced information on how to run MPI-based HPC applications as well as cutting-edge machine learning frameworks. Users will leave the tutorial with a solid foundational understanding of how to utilize containers with HPC resources through Singularity, as well as an in-depth knowledge to deploy custom containers on their own resources.

Room: Matterhorn 1
2:00 pm - 6:00 pm

Addressing the Skills Shortage in HPC - Strategies for Equity, Diversity and Inclusion

Addressing the Skills Shortage in HPC - Strategies for Equity, Diversity and Inclusion

Toni Collis (Collis-Holmes Innovations, Women High Performance Computing; Collis-Holmes Innovations), Kelly Nolan (Talent Strategy)

Hyperion research reports: ‘Nearly all (93%) of the HPC centers said it is “somewhat hard” or “very hard” to hire staff with the requisite skills’. The number and quality of research outputs in High Performance Computing (HPC), is directly dependent on the size, talent and skills of the HPC workforce. The HPC workforce is aritifically smaller than its full potential because of insufficient diversity. Equity, diversity and inclusion are laudable goals in their own right, and are necessary to increase the size of the available talent pool, but also improve business and research outcomes, such as increased profit, turnover and impact. However, achieving diversity is complex and difficult.

The HPC community has typically relied on generic ‘diversity in STEM/technology’ initiatives. Significant progress is being made in other STEM subjects, but HPC is not seeing the benefit..

Attendees will leave this tutorial with the key steps to producing a workable HPC targeted inclusion plan to build the talent pool in their organization including the business imperative, how to diagnose inclusion and diversity barriers in their organization and information on strategies to achieve cultural change and build workable solutions with a realistic probability of organizational buy-in.

Vendor Showdown

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Monday, June 17th

Room: Panorama 2
1:00 pm - 3:00 pm

Vendor Showdown 01

Introduction Vendor Showdown 01
Addison Snell, Rupak Biswas

Atos
Eric Eppe (Atos)

Oracle Cloud Infrastructure
Taylor Newill (Oracle Cloud Infrastructure)

Amazon Web Services
Brendan Bouffler (Amazon Web Services)

Dell EMC
Thierry Pellegrino (Dell EMC)

Cray

Steve Scott (Cray)

NEC Deutschland GmbH

Shintaro Momose (NEC Deutschland GmbH)

NetApp

Stan Skelton (NetApp)

Boston

David Power (BOSTON)

Microsoft Deutschland GmbH

Rob Walsh (Microsoft Corporation)

Panasas, Inc.

Dale Brantly (Panasas, Inc.)

Western Digital

Manfred Berger (Western Digital)

Voting Results & Awarding Vendor Showdown 01
Addison Snell, Rupak Biswas

Room: Panorama 3
1:00 pm - 3:10 pm

Vendor Showdown 02

Introduction Vendor Showdown 02
Dan Olds, Mark Parsons

Intel
Nash Palaniswamy (Intel)

Hewlett Packard Enterprise
Carlos Rojas (Hewlett Packard Enterprise)

Google LLC
Kevin Kissell (Google Inc.)

Mellanox Technologies

Gilad Shainer (Mellanox Technologies)

DDN Storage

Jan Heichler (DDN Storage)

Lenovo Data Center Group

Scott Tease (Lenovo)

IBM

Costas Bekas (IBM)

Samsung Semiconductor

Duc Nguyen (Samsung Semiconductor)

Inspur

Vangel Bojaxhi (Inspur)

Advania Data Centers

Gisli Kr (Advania Data Centers)

Fujitsu

Toshiyuki Shimizu (Fujitsu)

Marvell Semiconductor, Inc.: Innovative Alternative Architecture for Exascale Computing

Gopal Hegde (Marvell Semiconductor, Inc.)

Voting Results & Awarding Vendor Showdown 02

Dan Olds, Mark Parsons

Women in HPC Poster

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Tuesday, June 18th

Room: Areal
11:00 am - 4:45 pm

Research Posters + PhD Forum Posters + HPC in Asia Posters

Session Description: For a complete list of the Research Posters on display at ISC 2019, please refer to the
overview
of the Research Posters Session on Tuesday, June 18. For a complete list of the PhD Forum Posters on display at ISC 2019, please refer to the
overview
of the PhD Forum Posters Session on Monday, June 17. For a complete list of the HPC in Asia Posters on display at ISC 2019, please refer to the
overview
of the HPC in Asia Posters Session on Wednesday, June 19. For a complete list of the Woman in HPC Posters on display at ISC 2019, please refer to the
overview
of the Woman in HPC Posters on Tuesday, June 18.

Room: Areal
12:30 pm - 5:00 pm

Women in HPC Posters

(WHPC01) CHARMM Force Field Parameters for the Zn+ Center of 6-Pyruvoyl Tetrahydropterin Synthase Enzyme
Afrah Khairallah (Organization for Women in the Science for the Developing World, Rhodes University)

Drug discovery, development and finally commercialization is an expensive and time-consuming process.

Computer-aided drug development resolved this matter by allowing speedy identification of potential drug candidates with high binding affinity and selectivity towards selected metabolic targets. Therefore, decreasing the initial number of drug candidates to be lab tested and vastly reducing the time and cost of discovering effective drugs. In this study, computational approaches were used to aid in the discovery of new potential anti-malarial treatments and alternative metabolic targets. Appropriate Force Field (FF) parameters of the active site metal centres from the malaria parasite folate pathway enzyme 6-pyruvoyl tetrahydropterin synthase (PTPS), were derived quantum mechanically and then validated. We employed quantum mechanics (QM) and Potential Energy Surface scans (PESs) to generate the FF parameters and subsequently validated it using all atomics Molecular Dynamics (MD). The newly generated force field parameters will provide accurate and reliable MD simulations of the protein active site, which can improve the computer-aided attempts of identifying potential drug candidates for malaria treatment. The resources available at the Center for High-Performance Computing (Cape Town, South Africa) were utilized to perform the PESs using the Gaussian software package and all atomic MD simulations, using the Chemistry at HARvard Molecular Mechanics (CHARMM) MD-simulations packages, to investigate the validity of the integrated FF parameters. The use of HPC has accelerated and opened new perspectives to this process, allowing the use of parallel processor networks to study our large bio-molecule system. A problem which could not previously be dealt with.

(WHPC02) JASMIN: Super Data Cluster for Environmental Data Analysis

Cristina del Cano Novales (Science and Technology Facilities Council)

The JASMIN facility is a hybrid data cluster which delivers infrastructure for environmental science data. In this community, data sets are very often too large to be moved across networks. JASMIN puts together high performance storage and an efficient data analysis environment in one system – effectively bringing the processing to the data.

Group workspaces allow scientists to collaborate and share the data. The HPC Cluster and the virtualised cluster, connected to the storage with a high performance network, provide the analysis environment required to run models and algorithms on the data, which can be then evaluated before being stored in the JASMIN curated archive.

Cloud and virtualisation clusters provide the JASMIN tenants with the resources they require to host services, from data transfer in and out of JASMIN, to specific analysis environments, web servers, etc.

The need for this facility was identified in 2010, with initial funds secured in 2011 and with the first phase deployed at the beginning of 2012. Since then JASMIN has undergone major upgrades in 2014 and 2018, with another upgrade in progress for 2019. In this seven years, JASMIN has become a world leading environmental data analysis facility.

In this poster I will explain the JASMIN architecture, the services provided by this project and show some

examples of real-world science that JASMIN has helped deliver.

(WHPC03) Solving the Schrödinger Eigenproblem with PUMA

Clelia Albrecht (Fraunhofer Institute for Algorithms and Scientific Computing SCAI)

In this presentation we are concerned with the efficient approximation of the Schrödinger eigenproblem on general triclinic cells using an orbital-enriched flat-top partition of unity method (PUM).

To this end, we present the PUMA software framework, an MPI-parallel implementation of the flat-top PUM, which allows the user to access its full approximation power by employing arbitrary, problem-dependent enrichment functions. Furthermore, PUMA provides both a variational mass lumping scheme and a stability transformation that handles occurring stability problems in the resulting system matrices.

As an application example, we show the effective utilization of PUMA for the Schrödinger eigenproblem, where we observe a significant reduction of DOFs needed to obtain chemical accuracy compared to non-enriched approaches for model problems. Furthermore, due to the mass lumping scheme and stabilization we only have to solve a stable standard eigenvalue problem instead of a generalized eigenvalue problem. We show results obtained on the Drachenfels cluster at Fraunhofer SCAI. As more realistic physical problems can become very large, a more efficient parallel integration scheme as well as an optimized eigenvalue solver are interesting future challenges.

(WHPC04) Research Software Engineering enabling HPC

Anna Brown (Oxford e-Research Centre)

In a 2017 survey of UK-based researchers by the Software Sustainability Institute, 70% of respondents said that it would not be practical to conduct their work without research software and 56% said they developed their own software. However, modern HPC systems are often heterogeneous and massively parallel, leading to highly complex codes. In addition, specialised expertise in profiling and optimisation for a particular target architecture is often required to get close to the peak theoretical performance. Researchers are not guaranteed to have received software development or HPC training, and don't necessarily have time to spend on software maintenance.

The Research Software Engineering role combines training in software development with experience working in close collaboration with researchers. By having the creation of good software as their primary goal, RSEs in HPC are able to contribute lasting code that is fast, maintainable, well tested and easy to use.

We present two examples of RSE work enabling HPC. QuEST is a library for classical simulation of quantum circuits, a prime target for HPC due to memory requirements scaling exponentially with system

size. A fundamental design requirement was abstracting the complexity of HPC from the users; QuEST gives access to single CPU, multi-CPU and GPU parallelism through the same API. GS2 a simulator of turbulence in plasma physics, parallelised to run on O(10k) CPU cores. Profiling at scale was used to visualise the complex communication patterns inherent in the algorithm, informing the choice of optimal data distribution strategy.

(WHPC05) A Date with Data: How Time Series Information from Sensors & Logs is Revolutionizing HPC Data Center Operations at NERSC
Melissa Romanus Abdelbaky (Rutgers University, Lawrence Berkeley National Laboratory)

The National Energy Research Scientific Computing (NERSC) Center at the Lawrence Berkeley National Laboratory is home to two current Top500 high-performance computing systems, Cori (Cray XC40) and Edison (Cray XC30). The building, Shyh Wang Hall, and its data center are also home to the OMNI data collection project, which collects data from a variety of systems and sensors throughout the center, including building management systems, power infrastructure, temperature sensors, weather stations, system metrics and logs, seismometers, network routers, filesystems, particle counters, and more. The OMNI data collect contains over 500 billion records, totaling 117TB of data, and ingests new data at a rate of over 20,000 data points per second from these distributed, heterogeneous sources. In doing so, it provides a centralized location for the data that can be monitored, analyzed, and visualized with ease. By keeping more than two years worth of data online, researchers are able to ask new questions that were not possible before as well as revisit historical data for analyses if a future issue is discovered. In this poster, we explain the architecture of the OMNI data collection system as well as present four uses cases that demonstrate how the dataset led to valuable insights at NERSC. Key innovations from OMNI insights include increased energy-efficiency of the facility, critical preventative maintenance by adding a new tower water pump, and a cost savings of $2.5 million by determining that an additional mechanical substation was not necessary to support the new Perlmutter system.

Wednesday, June 19th

Room: Areal
8:30 am - 4:45 pm

Women in HPC Posters

Session Description: For a complete list of the Women in HPC Posters on display at ISC 2019, please refer to the
overview

of the Woman in HPC Posters Session on Tuesday, June 18.

Room: Areal
8:30 am - 5:00 pm

Research Posters + PhD Forum Posters + HPC in Asia Posters

Session Description: For a complete list of the Research Posters on display at ISC 2019, please refer to the
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of the Research Posters Session on Tuesday, June 18. For a complete list of the PhD Forum Posters on display at ISC 2019, please refer to the
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Workshop

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Thursday, June 20th

Room: Alabaster 1
9:00 am - 1:00 pm

3rd Workshop on HPC Computing in a Post Moore's Law World (HCPM) 2019

3rd Workshop on HPC Computing in a Post Moore's Law World (HCPM) 2019
Koen Bertels (TU Delft), Paul Carpenter (Barcelona Supercomputing Center), Phillippe Notton (European Processor Initiative), Christian Trott (Sandia National Laboratory), Martin Schulz (Technical University of Munich), Kentaro Sano (RIKEN), George Michelogiannakis (LBNL, Stanford University)

The emerging end of traditional MOSFET scaling has sparked a significant amount of research to preserve performance scaling of digital computing including drastically novel computational models. This workshop brings together leaders from different areas of this grand research thrust to educate the ISC community of current progress, future and immediate challenges, as well as the state of their research in the next 20 years. This year we invited speakers from key projects and institutions, representing thrusts from major funding agencies and countries. The subject space includes computational models, emerging technologies, as well as the programming and algorithmic impact. The workshop will feature a series of talks with ample time of discussion, as well as dedicated time at the end for a constructive discussion following the information that the invited speakers shared. The end goal of this workshop is to share our ideas about how HPC will look like in the next few decades, and how to adjust or affect upcoming changes.

Room: Alabaster 2
9:00 am - 1:00 pm

First International Workshop on Legacy Software Refactoring for Performance (REFAC'19)

First International Workshop on Legacy Software Refactoring for Performance (REFAC'19)

Benoit Marchand (New York University Abu Dhabi), Mauro Bianco (Swiss National Supercomputing Centre), Andreas Knüpfer (Technische Universität Dresden, ZIH), Didem Unat (Koç Univarsity), Nikolay A. Simakov (SUNY University at Buffalo, Center for Computational Research), Mohamed Wahib (TokyoTech Real World Big-Data Computation Open Innovation Laboratory, National Institute of Advanced Industrial Science and Technology (AIST)), Jens Domke (RIKEN Center for Computational Science), Artur Podobas (RIKEN Center for Computational Science)

"The first International Workshop on Legacy Software REFACtoring for Performance" is the first event of its kind that is dedicated to the much needed shift in focus from hardware to software to achieve performance gains. Unfortunately, we are no longer seeing the consistent technology scaling that Moore observed. Instead, the technology scaling has significantly slowed down, and is expected to continue only for a few more years. The workshop focuses on maintainable and architecture-oblivious software optimizations. With this, we mean optimizations that are transferable across computer systems and architectures, and that remain portable and pose little to none maintenance costs; hence, we focus our discussions and studies less on code migrations and porting efforts, since those topics are already very well covered by other forums.

Room: Flint
9:00 am - 1:00 pm

Women in HPC: Diversifying the HPC Community and engaging male allies

Women in HPC: Diversifying the HPC Community and engaging male allies
Jo Adegbola (Amazon Web Services), Brendan Bouffler (Amazon Web Services), Theresa Best (HackerstolzWomen), Kelly Nolan (Talent Strategy), Helena Liebelt (Intel), Laura Schulz (Leibniz Supercomputing Center), Martina Naughton (IBM), Mozhgan Kabiri Chimeh (The University of Sheffield), Toni Collis (Collis-Holmes Innovations, Women High Performance Computing; Collis-Holmes Innovations), Mozhgan Kabiri chimeh (University of Sheffield), Toni Collis (Appentra Solutions S.L., Collis-Holmes Innovations)

The tenth international Women in HPC workshop will be held at ISC19, Frankfurt, Germany. This workshop provides leaders and managers in the HPC community with methods to improve diversity and also to provide early career women with an opportunity to develop their professional skills and profile. Following the overwhelming success of the 2018 WHPC workshops we will once again discuss methods and steps that can be taken to address the under-representation of women, in particular by discussing the following topics: Being part of the solution: instructions for advocates and allies Putting in place a framework to help women take leadership positions Building mentoring programmes that work effectively for women. We will also provide opportunities aimed at promoting and providing women with the skills to

thrive in HPC including: Posters and lightning talks by women working in HPC Short talks on: dealing with poor behaviour at work and how to help avoid it getting you down, how to deal with negative feedback, how to build writing into your daily routine and why it matters, etc.

Room: Kilobyte
9:00 am - 1:00 pm

Second Workshop on the Convergence of Large Scale Simulation/HPC and Artificial Intelligence

Second Workshop on the Convergence of Large Scale Simulation/HPC and Artificial Intelligence
Azalia Mirhoseini (Google Brain), Tal Ben-Nun (ETH Zurich), Menno Veerman (Wageningen University and Research), Alper Yegenoglu (Forschungszentrum Juelich), Mathis Bode (RWTH Aachen), Nico Hoffmann (HZDR), Christoph Martin Angerer (NVIDIA), Axel Koehler (NVIDIA)

In 2016, an artificial intelligence (AI) named AlphaGo became the first machine to beat a human 9-dan professional Go player on a full-sized board. Since then, AI has proven its potential to revolutionize our social life, how we live, work, learn, discover, and communicate. But does AI also have the potential to fundamentally change how we do science? The recent stream of publications suggests it may, but there is still much work to be done before AI can enter the day-to-day toolbox of scientists.

This is the second iteration of this workshop, where we will discuss ways that Deep Learning and Artificial Intelligence can be combined with traditional HPC to accelerate the pace of scientific discovery from High Energy Physics to Life Sciences and Healthcare.

The traditional paradigm uses large scale simulation at the core, where data analytics are used for pre and post processing of the data. In the new paradigm, AI and large scale simulation will be applied on a more cooperative basis where the strengths of each converge to form a powerful new tool for science. In this workshop we will discuss both paradigms, traditional and new, but put a focus on the new paradigm.

Room: Megabyte
9:00 am - 1:00 pm

Workshop on HPC Education and Training for Emerging Technologies

Workshop on HPC Education and Training for Emerging Technologies

Alan O'Cais (Forschungszentrum Juelich GmbH), Peter Steinbach (Scionics Computer Innovation GmbH), Scott Lathrop (NCSA - University of Illinois), Robert Panoff (Shodor Education Foundation, Inc.), Jennifer Houchins (Shodor Education Foundation, Inc.), Aaron Weeden (Shodor Education Foundation, Inc.), Julian Martin Kunkel (University of Reading), Jean-Thomas Acquaviva (DDN), Kai Himstedt (University of Hamburg), Weronika Filinger (The University of Edinburgh), Anja Gerbes (Goethe-Universität), Lev Lafayette (The University of Melbourne), Tim Powell (Hartree Centre STFC), James Pyle (The University of Sheffield), Mozhgan Kabiri Chimeh (The University of Sheffield), Chris Bording (IBM), Kwai Wong (Univ. Tennessee), Stanimire Tomov (Univ. Tennessee), Jack Dongarra (Univ. Tennessee), Frédéric Parienté (NVIDIA), Fernanda Foertter (NVIDIA), Michael Croucher (NAG), Nitin Sukhija (Slippery Rock University of Pennsylvania), Nia Alexandrov (STFC Hartree Centre), Scott Lathrop (University of Illinois)

HPC is central for empowering progress in diverse scientific and non-scientific domains. A myriad of technologies in the post peta-scale computing demand a significantly greater degree of parallelism than we currently observe. The rapid advancement of new HPC technologies has facilitated the convergence of Artificial Intelligence (AI), Big Data Analytics, and the HPC platforms to solve complex, large-scale, real-time analytics and applications for scientific and non-scientific fields. As we move towards exascale, the convergent computing platforms along with a paradigm shift in the programming applications for them provide both challenges and opportunities, for cyberinfrastructure facilitators and educators to prepare and support a diverse community of professionals to utilize evolving HPC, equipping them to solve complex scientific, engineering, and technological problems. The HETET19 workshop is coordinated by ACM SIGHPC-Education Chapter and fosters collaborations among practitioners to explore strategies enhancing computational, data-enabled, AI and HPC educational needs. Attendees will discuss approaches for developing and deploying HPC education and training, and keeping pace with the rapid technological advances: collaborative online learning tools, technology solutions supporting HPC, Accelerated Analytics, and AI applications. The workshop will highlight: methods for conducting effective HPC education and training for emerging technologies; promote HPC educators community; disseminate best practices.

Room: Platinum 2
9:00 am - 6:00 pm

Deep Learning for Science

Deep Learning for Science
Sofia Vallecorsa (CERN), Zhao Zhang (Texas Advanced Computing Center), Valeriu Codreanu (SURFsara), Ian T. Foster (University of Chicago, Argonne National Laboratory)

The Deep Learning (DL) for Science workshop provides a forum for practitioners working on any and all aspects of DL for science and engineering in the High Performance Computing (HPC) context to present their latest research results and development, deployment, and application experiences. The general theme of this workshop series is the intersection of DL and HPC; the theme of this particular workshop is the applications of DL methods in and science and engineering: novel uses of DL methods, e.g., convolutional neural networks (CNN), recurrent neural networks (RNN), generative adversarial networks (GAN), and reinforcement learning (RL), in the natural sciences, social sciences, and engineering, to encompass innovative applications of DL in traditional numerical computation. Its scope encompasses application development in scientific scenarios using HPC platforms; DL methods applied to numerical simulation; fundamental algorithms, enhanced procedures, and software development methods to enable scalable training and inference; hardware changes with impact on future supercomputer design; and machine deployment, performance evaluation, and reproducibility practices for DL applications with an emphasis on scientific usage. This workshop will be centered around published papers. Submissions will be peer-reviewed, and accepted papers will be published as part of the Joint Workshop Proceedings by Springer.

Room: Gold 1
9:00 am - 6:00 pm

X86, ARM, GPUs! Today's Programming Environment for the Complex, Many-choice Platforms in HPC

X86, ARM, GPUs! Today's Programming Environment for the Complex, Many-choice Platforms in HPC

Luiz DeRose (Cray Inc), C.J. Newburn (NVIDIA), Bronis de Supinski (LLNL), Michael Schulte (AMD), Patrick Wohlschlegel (ARM), James Cownie (Intel), Mitsuhisa Sato (Riken), Oscar Hernandez (ORNL), Christian Trott (SNL), Jeff Hittinger (LLNL), Simon McIntosh-Smith (University of Bristol), John Linford (ARM), Heidi Poxon (Cray Inc), Luiz DeRose (Cray Inc)

A key component for a fast and balanced supercomputer is the programming environment. The scale and complexity of current and future high-end systems brings a new set of challenges for application developers. The technology changes in the supercomputing industry, coupled with the emergence of new processor and accelerator architectures, force computational scientists to face new critical system characteristics that will significantly impact the performance and scalability of applications. With the next generation of supercomputers, application developers need sophisticated compilers, tools, libraries, and adaptive runtime systems that can help maximize programmability with low porting and tuning efforts, while not losing sight of performance portability across a wide range of processors and architectures. Application developers need programming environments that can address, as well as hide, the issues of

scale and complexity of high-end HPC systems. This workshop will focus on the programming environments that target the emerging processors and accelerators for the exascale class of supercomputers. It will have presentations from industry, as well as end-user experiences with the available programming environment. The keynote will discuss the programming environment needs for the US DOE CORAL systems and the new features in OpenMP 5.0 that are most expected to impact its use.

Room: Gold 2
9:00 am - 6:00 pm

The First Annual Workshop for HPC PowerStack

The First Annual Workshop for HPC PowerStack
Martin Schulz (Technical University of Munich, Leibniz-Rechenzentrum), Siddhartha Jana (Energy Eff HPC Working Group, Intel), Martin Schulz (Technical University of Munich, Leibniz-Rechenzentrum), Masaaki Kondo (University of Tokyo), Siddhartha Jana (Energy Efficient HPC Working Group, Intel)

While there exist several standalone efforts that attempt to tackle exascale power challenges, the majority of the implemented techniques have been designed to meet site-specific needs or optimization goals. Specifications such as PowerAPI and Redfish provide high-level power management interfaces for accessing power knobs. However, these stop short of defining which software components should actually be involved, and how should they interoperate with each other in a cohesive and coordinated stack. We believe coordination is critical for avoiding underutilization of system Watts and FLOPS.

This interactive workshop brings together vendors, labs, and academic researchers to discuss an emerging community effort to develop a software stack for system-wide power optimization. The HPC PowerStack effort is the first to identify what power optimization software actors are needed; how they interoperate to achieve stable, synchronized optimization; and how to glue together existing open source projects to engineer a cost-effective but cohesive, cross-platform power stack implementation.

Room: Gold 3
9:00 am - 6:00 pm

Arm HPC User Group (AHUG) 2019

Arm HPC User Group (AHUG) 2019

Giri Chukkapalli (Marvell), Pak Lui (Huawei), Larry Kaplan (Cray), Phillippe Notton (CEA), Andy Warner (HPE), Stephen Poole (LANL), Guillaume Colin de Verdiere (CEA), Ashok Bhat (Arm), Miquel Tairum-Cruz (Arm), Mitsuhisa Sato (RIKEN), Shinji Sumimoto (Fujitsu), Dirk Pleiter (Jülich Research Center), Mark Wilkinson (University of Leicester and Edinburgh Parallel Computing Center), Mark Parsons (University of Leicester and Edinburgh Parallel Computing Center), Rob Hoekstra (Sandia National Labs), Seid Derraji (Atos), Miquel Moreto (Barcelona Supercomputing Center), Simon McIntosh-Smith (University of Bristol), tbd tbd (Arm), Vladimir Alves (NGD Systems), Viraj R Paropkari (Xilinx), Thorsten Queckboerner (ESI), Greg Samonds (ESI), Gilad Shainer (Mellanox), Jonathan Beard (Arm Research), Roxana Rusitoru (Arm Research), Jeffrey Young (Georgia Tech University), Oscar Hernandez (Oak Ridge National Lab)

The Arm HPC Users Group (AHUG) will enable attendees to take in technical presentations by fellow applications programmers and tool authors who are currently using the Arm platform.

AHUG is about sharing experiences and knowledge. Attendees will gain from the first-hand knowledge of experienced scientific application programmers writing for the Arm platform, including topics such as: optimizing for 64-bit Arm, memory systems, scalability and vectorisation.

Content specifically focuses on HPC applications and cross-over/emerging application areas such as machine learning, deep learning, bioinformatics, and analytics.

Room: Basalt
9:00 am - 6:00 pm

HPC I/O in the Data Center

HPC I/O in the Data Center
Patrick Widener (Sandia National Laboratries), Jay Lofstead (Sandia National Laboratories), Sandro Fiore (CMCC), Julian Kunkel (University of Reading), Jorji Nonaka (Riken), Vinay Gaonkar (KMesh), Alberto Chiusole (eXact lab srl), Adrian Jackson (Edinburgh Parallel Computing Centre (EPCC)), Glenn Lockwood (Lawrence Berkeley National Laboratories), Eugen Betke (Deutsches Klimarechenzentrum (DKRZ)), Eloise Billa (CEA), Jean-Thomas Acquaviva (DDN), Oussama Elhamer (Univ. Bretagne Occidentale), Jianshen Liu (University of California, Santa Cruz), Julian Kunkel (University of Reading), Jay Lofstead (Sandia National Laboratory)

Managing scientific data at large scale is challenging for scientists but also for the host data center. To effectively manage the data load within a data center, I/O experts must understand how users expect to use these new storage technologies and what services they should provide in order to enhance user

productivity. We seek to ensure a systems-level perspective is included in these discussions.

The HPC-IODC workshop is a forum to present and discuss work that addresses the storage challenge from a unique perspective, moving the focus from the application-centric perspective to the perspective of data centers and operators. In the workshop, we bring together I/O experts from data centers and application workflows to share current practices for scientific workflows, issues, and obstacles for both hardware and the software stack, and R&D to overcome these issues. We accepted research papers that are state-of-the-practice or research-oriented but specifically focused on I/O in the datacenter. The sessions are jointly organized with the Workshop on Performance and Scalability of Storage Systems (WOPSSS) hosting performance-oriented research papers. Detailed information is provided on the web page.

Room: Gigabyte
9:00 am - 6:00 pm

Fourth Workshop on Performance Portable Programming Models for Accelerators (P3MA)

Fourth Workshop on Performance Portable Programming Models for Accelerators (P3MA)
Mitsuhisa Sato (RIKEN), Simon McIntosh-Smith (University of Bristol), Veronica Melesse Vergara (Oak Ridge National Laboratory), Nabeeh Jum'Ah (University of Hamburg), Istvan Reguly (Pázmány Péter Catholic University), Sunita Chandrasekaran (University of Delaware), Swaroop Pophale (Oak Ridge National Laboratory)

Performance portable approaches and implementations are becoming increasingly crucial for the application developers to make the best use of modern HPC architectures. With diverging architectural designs, it can be a challenge to develop high-level abstractions that can expose all the rich features of the hardware to the programmer, especially with the introduction of heterogeneous architectures. This workshop will provide a forum to bring together researchers and developers to discuss community's proposals and solutions to performance portability.

Room: Matrix
9:00 am - 6:00 pm

5th Annual High Performance Container Workshop

5th Annual High Performance Container Workshop
Abdulrahman Azab Mohamed (University of Oslo, Partnership for Advanced Computing in Europe (PRACE)), Christian Kniep (Docker Inc.), Shane Canon (Lawrence Berkeley National Lab), Eduardo Arango (Sylabs), Valentin Rothberg (RedHat), Lucas Benedicic (CSCS Swiss National Supercomputing Centre), Akihiro Suda (NTT Corp), Parav Pandit (Mellanox Technologies), Arthur Petitpierre (AWS), CJ Newburn (NVIDIA), Christian Kniep (Docker Inc.), Abdulrahman Azab Mohamed (University of Oslo, Partnership for Advanced Computing in Europe (PRACE))

Linux Containers continue to gain momentum within data centers all over the world. They are able to benefit legacy infrastructures by leveraging the lower overhead compared to traditional, hypervisor-based virtualization. But there is more to Linux Containers, which this workshop will explore. Their portability, reproducibility and distribution capabilities outclass all prior technologies and disrupt former monolithic architectures, due to sub-second life cycles and self service provisioning.

This workshop will outline the current state of Linux Containers, what challenges are hindering the adoption in HPC/BigData and how containers can foster improvements when applied to the field of HPC, Big Data and AI in the mid- and long-term. By dissecting the different layers within the container ecosystem (runtime, supervision, engine, orchestration, distribution, security, scalability) this workshop will provide a holistic and a state-of-the-container overview, so that participants can make informed discussions on how to start, improve or continue their container adoption.

Room: Ampere
9:00 am - 6:00 pm

Fifth International Workshop on Communication Architectures for HPC, Big Data, Deep Learning and Clouds at Extreme Scale

Fifth International Workshop on Communication Architectures for HPC, Big Data, Deep Learning and Clouds at Extreme Scale
Steve Scott (Cray), Dror Goldenberg (Mellanox Technologies), Yuichiro Ajima (Fujitsu Coporation), Taeyoung Hong (KISTI), Felix Schürmann (EPFL), Hirotaka Ogawa (AIST), Brian Barrett (Amazon), Evan Burness (Microsoft), Ron Brightwell (Sandia National Laboratory), Nikolaos Chrysos (tba), Hari Subramoni (The Ohio State University), Dhabaleswar Panda (The Ohio State University)

Extreme Scale computing in HPC, Big Data, Deep Learning and Clouds are marked by multiple-levels of hierarchy and heterogeneity ranging from the compute units (many-core CPUs, GPUs, APUs etc) to storage devices (NVMe, NVMe over Fabrics etc) to the network interconnects (InfiniBand, High-Speed

Ethernet, Omni-Path etc). Owing to the plethora of heterogeneous communication paths with different cost models expected to be present in extreme scale systems, data movement is seen as the soul of different challenges for exascale computing. On the other hand, advances in networking technologies such as NoCs (like NVLink and Stormlake), emergence of new I/O interface architecture standards (CCIX, Gen-Z, CAPI etc), and RDMA enabled networks and the likes are constantly pushing the envelope of research in the field of novel communication and computing architectures for extreme scale computing. The goal of this workshop is to bring together researchers and software/hardware designers from academia, industry and national laboratories who are involved in creating network-based computing solutions for extreme scale architectures. The objectives of this workshop will be to share the experiences of the members of this community and to learn the opportunities and challenges in the design trends for exascale communication architectures.

Room: Volt
9:00 am - 6:00 pm

14th Workshop on Virtualization in High-Performance Cloud Computing

14th Workshop on Virtualization in High-Performance Cloud Computing
Brian Barrett (Amazon), Tim Bell (CERN), Romeo Kienzler (IBM), Taylor Newill (Oracle), Andrey Kudryavtsev (Intel), Benzi Galili (ScaleMP), Simon Kuenzer (NEC Laboratories Europe GmbH), Michael Alexander (University of Vienna, Enpulsion), Anastassios Nanos (SunLight.io), Andrew Younge (Sandia National Laboratories)

The Workshop on Virtualization in High-Performance Cloud Computing (VHPC) aims to bring together researchers and industrial practitioners facing the challenges posed by virtualization in order to foster discussion, collaboration, mutual exchange of knowledge and experience, enabling research to ultimately provide novel solutions for virtualized computing systems of tomorrow.

Room: Candela
9:00 am - 6:00 pm

WOIV'19: 4th International Workshop on In Situ Visualization

WOIV'19: 4th International Workshop on In Situ Visualization
Steffen Frey (University of Stuttgart), Peter Messmer (NVIDIA), Thomas Theussl (KAUST)

Large-scale HPC simulations with their inherent I/O bottleneck have made in situ an essential approach for data analysis. The `"International Workshop on In Situ Visualization" provides a venue for speakers to share practical experience with in situ visualization approaches. We encourage contributed talks on methods and workflows that have been applied in this field. For this 4th edition of the workshop, we again encourage submissions on approaches that either did not work at all or did not live up to their expectations. We therefore expect to get first-hand reports on lessons learned. In particular, we also encourage researchers to discuss approaches that didn't achieve the intended goal along with insights derived from the process. Our goal is to appeal to a wide-ranging audience of visualization scientists, computational scientists, and simulation developers, who closely collaborate in order to develop, deploy, and maintain in situ visualization approaches on HPC infrastructures. We hope to provide practical take-away techniques and insights that serve as inspiration for attendees to implement or refine in their own HPC environments and to avoid pitfalls.

Room: Lux
9:00 am - 6:00 pm

Third HPC Applications in Precision Medicine

Third HPC Applications in Precision Medicine
Kerstin Kleese van Dam (Brookhaven National Laboratory), Paul Macklin (Indiana University), Fangfang Xia (Argonne National Laboratory), Gard Thomassen (University of Oslo), Eric Stahlberg (Frederick National Laboratory for Cancer Research), Jan Nygard (The Cancer Registry of Norway), Christian Bolliger (ETH Zurich), Thomas Steinke (Zuse Institute Berlin), Sunita Chandrasekaran (University of Delaware)

High-performance computing has become central to the future success of precision medicine. Catalyzed by the dramatic increase in the volume of research and clinical data available through sequencing and advanced imaging techniques, clinical data available through medical records and mobile health devices, research data from automated platforms, combined with molecular simulations and the rapid adoption of deep learning approaches has created a convergence shaping the frontiers of computing and precision medicine. New approaches to drug discovery, data sharing, aggregation and safeguards, use of machine learning models in research and clinical contexts has identified new challenges and opportunities in these rapidly evolving frontiers. The Third HPC Applications in Precision Medicine workshop aims to bring together the computational and life sciences communities to share experiences, examine current challenges, and discuss future opportunities for shaping the future for HPC applications in precision medicine.

Room: Lava 1, 2
9:00 am - 6:00 pm

International Workshop on OpenPOWER for HPC 2019

International Workshop on OpenPOWER for HPC 2019
Kaushik Velusamy (University of Maryland, Baltimore County), Alexandre Castellane (IBM France), Arenaz Manuel (Appentra and University of Coruna), Ahmad Hesam (Delft University of Technology), Kawthar Shafie Khorassani (The Ohio State University), John Ossyra (University of Tennessee Knoxville), Andreas Herten (Forschungszentrum Juelich / Juelich Supercomputing Centre), Veronica Vergara Larrea (Oak Ridge National Laboratory), Ajay Arasanipalai (HLC international school), Dirk Pleiter (Juelich Supercomputing Centre), Jack Wells (ORNL), Jesus Labarta (UPC & BSC)

The OpenPOWER Foundation has been established as a technology organization that enables collaboration between different technology providers resulting in new solutions for HPC and HPDA solutions. Systems with nodes based on IBM POWER9 processors with NVLink-attached NVIDIA V100 GPUs provide about 18% of the performance of the current Top500 systems. CAPI and OpenCAPI are receiving increasing attention as interface for attaching other types of accelerators like FPGAs.

This workshop will provide a venue for HPC and extreme-scale data technology experts as well as for application developers to present results obtained on OpenPOWER technologies. The latest advances in OpenPOWER addressing challenges in system architecture, networking, memory designs, exploitation of accelerators, programming models, and porting applications in machine learning, data analytics, modeling and simulation are of current interest within the HPC community and this workshop. In particular, the use of the new NVLink technology as well as the use of the CAPI/OpenCAPI technology is of interest. Closely related topics also include OpenACC, OpenMP, OpenSHMEM, MPI, developer and performance tools, etc. for the OpenPOWER ecosystem.

This would be the 4th edition of the workshops. All IWOPH workshops organised since ISC'16 were well attended. We observe an increasing number of paper submission.

Room: Alabaster 2
2:00 pm - 6:00 pm

Scalable Data Analytics in Scientific Computing

Scalable Data Analytics in Scientific Computing

Dhabaleswar Panda (The Ohio State University), Kushal Datta (Intel), Valentin Kozlov (Karlsruhe Institute of Technology), Kai Krajsek (Juelich Supercomputing Centre), Stanimire Tomov (University of Tennessee), Hartwig Anzt (Karlsruhe Institut für Technologie, Steinbuch Centre for Computing)

With increasing importance of statistical inference methods and their use at large cloud and warehouse-scale computing industry, we propose a workshop called Scalable Data Analytics in Scientific Computing (SDASC). It will feature automated data analysis efforts on the convergence of computational science, HPC, and large scale data analytics and inference. The workshop will focus on integration of the HPC techniques and statistical learning and related tasks into modern computational software stack.

The half-day workshop will gather experts from the computational science, HPC, and machine learning. The committee members are recognized in their respective fields as experts of note and will assure fulfilment of the goals of the workshop outlined below.

This workshop could also be considered as a complementary event to the Machine Learning Learning Day slated to take place at ISC 2019.

Room: Flint
2:00 pm - 6:00 pm

Second Workshop on Interactive High-Performance Computing

Second Workshop on Interactive High-Performance Computing
John Ossyra (University of Tennessee, Knoxville), Robert Settlage (Virginia Tech), Tuomas Eerola (Techila Technologies), Jack Wells (Oak Ridge National Laboratory), Nick Brown (Edinburgh Parallel Computing Centre (EPCC)), Benjamin Robbins (Cray), Albert Reuther (Massachusettes Institute of Technology, Lincoln Laboratory), Michael Ringenburg (Cray Inc.), Michael Ringenburg (Cray Inc.)

Interactive exploration of large data sets, interactive preparation and debugging of large-scale scientific simulations, in-situ visualization, and application steering are compelling scenarios for exploratory science, design optimizations, or signal processing. However, a range of technical, organizational and sociological challenges must be overcome to make these workflows mainstream: What simulation scenarios or problem domains can benefit most from interactivity? How can we simplify the toolchain? What center policies are needed to support highly interactive workflows? The goal of this workshop is to bring together domain scientists, tool developers, and HPC center administrators to identify the scientific impact and technical challenges of highly interactive access to HPC resources.

Room: Kilobyte
2:00 pm - 6:00 pm

Numerical Reproducibility at Exascale 2019

Numerical Reproducibility at Exascale 2019

Michael Mascagni (Florida State University, NIST), Walid Keyrouz (NIST)

Reproducibility is an important concern in all areas of computation. As such, computational and numerical reproducibility is receiving increasing interest from a variety of parties who are concerned with different aspects of computational reproducibility. Numerical reproducibility encompasses several concerns including the sharing of code and data, as well as reproducible numerical results which may depend on operating systems, tools, levels of parallelism, and numerical effects. In addition, the publication of reproducible computational results motivates a host of computational reproducibility concerns that arise from the fundamental notion of reproducibility of scientific results that has normally been restricted to experimental science.

The workshop is meant to address the scope of the problems of computational reproducibility in HPC in general, and those anticipated as we scale up to Exascale machines in the next decade. The participants of this workshop will include government, academic, and industry stakeholders; the goals of this workshop are to understand the current state of the problems that arise, what work is being done to deal with this issues, and what the community thinks the possible approaches to these problem are.

Room: Megabyte
2:00 pm - 6:00 pm

Using FPGAs to Accelerating HPC and Data Analytics on Intel-Based Systems

Using FPGAs to Accelerating HPC and Data Analytics on Intel-Based Systems

Christian Plessl (Universität Paderborn), Kentaro Sano (RIKEN Center for Computational Science), José Roberto Alvarez (Intel Corporation), Herman Lam (University of Florida), Nick Brown (The University of Edinburgh), Erik Debenedictis (Sandia National Laboratories), Taisuke Boku (University of Tsukuba), David E. Martin (Argonne National Laboratory), Nalini Kumar (Intel), Thomas Steinke (Zuse Institute Berlin), Estela Suarez (Forschungszentrum Jülich / Jülich Supercomputing Centre)

FPGAs are able to improve performance, energy efficiency and throughput by boosting computation, I/O and communication operations in HPC, data analytics (DA), and machine learning (ML) workloads and

thus complement the general-purpose Intel Xeon CPUs.

Recent innovations in hardware and software technologies make FPGAs increasingly attractive for HPC and DA workloads. The technological progress includes new FPGA SoCs featuring multi-core CPUs, increasingly larger reconfigurable logic and many hardened floating-point DSP blocks, improved compiler technologies capable of targeting heterogeneous systems, and tools for transforming intermediate representation objects into a hardware description language. Parallel programming models and standard APIs (OpenCL, OpenMP) are evolving to address the programmability aspect, better expressing data parallelism and data dependencies.

The workshop will bring together software developers and technology experts to share challenges, experiences and best practices around the integration and use of FPGA devices in HPC and DA/ML workloads in an Intel-based HPC ecosystem. The workshop will cover strategies for migrating workloads onto FPGAs, performance comparison with GPUs and CPUs, aspects of productivity, performance portability, and scalability.

The keynote will give an overview and outlook of the near future of the use of FPGAs and GPUs in the Intel HPC ecosystem.